SECTION 10
DRAM CONTROLLER

10.1 INTRODUCTION

The DRAM controller (DRAMC) provides a glueless interface between the ColdFire core and external DRAM. The DRAMC supports two banks of DRAM. Each DRAM bank can be from 128 kbyte to 256 Mbyte, in widths of 8, 16, or 32 bits. Two row address strobe ($\overline{RAS}$[1:0]) signals are provided externally to access the two DRAM banks. Data byte lanes are enabled using the four column address strobe ($\overline{CAS}$[3:0]) signals. The DRAM write ($\overline{DRAMW}$) signal indicates if the DRAM transfer is a read or a write. The DRAMC handles address multiplexing internally, allowing for a glueless DRAM interface. The DRAMC has an internal refresh timer that generates $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. You can program $\overline{RAS}$ and $\overline{CAS}$ waveform timing and refresh rates. Alternate master use of the DRAMC for accessing the DRAM banks is also supported.

10.1.1 Features

The following list summarizes the key DRAMC features:

- Supports two banks of DRAM
- Supports Normal Mode, Fast Page Mode, and Burst Page Mode
- Supports EDO DRAMs
- Supports glueless row address/column address multiplexing
- Programmable $\overline{RAS}$ and $\overline{CAS}$ timings
- Programmable refresh timer for $\overline{CAS}$-before-$\overline{RAS}$ refresh
- Supports alternate master use of the DRAMC

10.2 DRAM CONTROLLER I/O

10.2.1 Control Signals

The DRAMC has seven control signal signals: $\overline{CAS}$[0], $\overline{CAS}$[1], $\overline{CAS}$[2], $\overline{CAS}$[3], $\overline{RAS}$[0], $\overline{RAS}$[1], and $\overline{DRAMW}$.

10.2.1.1 ROW ADDRESS STROBES ($\overline{RAS}$[0], $\overline{RAS}$[1]). These active-low output signals provide control for the row address strobe ($\overline{RAS}$) input pins on industry-standard DRAMs. There is one $\overline{RAS}$ output for each DRAM bank: $\overline{RAS}$[0] controls DRAM bank 0 and $\overline{RAS}$[1] controls DRAM bank 1. $\overline{RAS}$ timing can be customized to match the specifications of the DRAM being used by programming the DRAMC Timing Register (see **Section 10.4.2.2 DRAM Controller Timing Register (DCTR)**).

10.2.1.2 COLUMN ADDRESS STROBES ($\overline{CAS}$[0], $\overline{CAS}$[1], $\overline{CAS}$[2], $\overline{CAS}$[3]). These active-low output signals provide control for the column address strobe ($\overline{CAS}$) input pins on industry-standard DRAMs. The $\overline{CAS}$ signals are used to enable data byte lanes: $\overline{CAS}$[0] controls access to D[31:24], $\overline{CAS}$[1] to D[23:16], $\overline{CAS}$[2] to D[15:8], and $\overline{CAS}$[3] to D[7:0]. $\overline{CAS}$[3:0] should be used for a 32-bit wide DRAM bank, $\overline{CAS}$[1:0] for a 16-bit wide DRAM bank, and $\overline{CAS}$[0] for an 8-bit wide DRAM bank. Table 10-1 shows which $\overline{CAS}$ signals are asserted based on the operand size, the DRAM port size and the address bits A[1:0]. For DRAM transfers SIZ[1:0] will always match the operand size.

Table 10-1. $\overline{CAS}$ Assertion

OPERAND SIZE	PORT SIZE	SIZ[1]	SIZ[0]	A[1]	A[0]	$\overline{CAS}$[0]	$\overline{CAS}$[1]	$\overline{CAS}$[2]	$\overline{CAS}$[3]
						D[31:24]	D[23:16]	D[15:8]	D[7:0]
BYTE	8-BIT	0	1	0	0	0	1	1	1
				0	1	0	1	1	1
				1	0	0	1	1	1
				1	1	0	1	1	1
	16-BIT	0	1	0	0	0	1	1	1
				0	1	1	0	1	1
				1	0	0	1	1	1
				1	1	1	0	1	1
	32-BIT	0	1	0	0	0	1	1	1
				0	1	1	0	1	1
				1	0	1	1	0	1
				1	1	1	1	1	0
WORD	8-BIT	1	0	0	0	0	1	1	1
				0	1	0	1	1	1
				1	0	0	1	1	1
				1	1	0	1	1	1
	16-BIT	1	0	0	0	0	0	1	1
				1	0	0	0	1	1
	32-BIT	1	0	0	0	0	0	1	1
				1	0	1	1	0	0
LONG WORD	8-BIT	0	0	0	0	0	1	1	1
				0	1	0	1	1	1
				1	0	0	1	1	1
				1	1	0	1	1	1
	16-BIT	0	0	0	0	0	0	1	1
				1	0	0	0	1	1
	32-BIT	0	0	0	0	0	0	0	0

Table 10-1. $\overline{CAS}$ Assertion (Continued)

OPERAND SIZE	PORT SIZE	SIZ[1]	SIZ[0]	A[1]	A[0]	$\overline{CAS}$[0] D[31:24]	$\overline{CAS}$[1] D[23:16]	$\overline{CAS}$[2] D[15:8]	$\overline{CAS}$[3] D[7:0]
LINE	8-BIT	1	1	0	0	0	1	1	1
				0	1	0	1	1	1
				1	0	0	1	1	1
				1	1	0	1	1	1
	16-BIT	1	1	0	0	0	0	1	1
				1	0	0	0	1	1
	32-BIT	1	1	0	0	0	0	0	0

$\overline{CAS}$ timing can be customized to match the specifications of the DRAM by programming the DRAM Controller Timing Register (see **Section 10.4.2.2 DRAM Controller Timing Register (DCTR)**).

10.2.1.3 DRAM WRITE ($\overline{DRAMW}$). This active-low output signal is asserted during DRAM write cycles, and negated during DRAM read cycles. The $\overline{DRAMW}$ signal is negated during refresh cycles.The $\overline{DRAMW}$ signal is provided in addition to the R/$\overline{W}$ signal to allow refreshes to occur during nonDRAM cycles (regardless of the state of the R/$\overline{W}$ signal). The R/$\overline{W}$ signal indicates the direction of all bus transfers, while $\overline{DRAMW}$ is only valid during DRAM transfers.

10.2.2 Address Bus

The address bus includes 24 dedicated address signals, A[23:0], and supports as many as four additional configurable address signals, A[27:24] (refer to **Section 7.3.2.10 Pin Assignment Register (PAR)**). The DRAM address will appear only on the pins configured to be address signals. The maximum size of DRAM that can be connected to each bank is limited by the number of address signals available (see Table 10-2).

Table 10-2. Maximum DRAM Bank Sizes

AVAILABLE ADDRESS SIGNALS	MAXIMUM DRAM SIZE
A[23:0]	16 Mbyte
A[24:0]	32 Mbyte
A[25:0]	64 Mbyte
A[26:0]	128 Mbyte
A[27:0]	256 Mbyte

For transfers initiated by the ColdFire core, the DRAMC outputs both the row address and the column address, allowing the address bus to be directly connected to external DRAM. The internal address multiplexing can be selectively enabled for transfers initiated by an alternate master by programming the DAEM bit in the DCTR (see **Section 10.4.2.2 DRAM Controller Timing Register (DCTR)**).

10.2.3 Data Bus

The DRAM banks can be configured to be 8, 16, or32-bits wide. A 32-bit port must reside on data bus bits D[31:0], a 16-bit port must reside on data bus bits D[31:16] and an 8-bit port must reside on data bus bits D[31:24]. This requirement ensures that the MCF5206 correctly transfers valid data to 8, 16 and 32-bit ports. Figure 10-1 illustrates the connection of the data bus to 8-, 16-, and 32-bit ports.

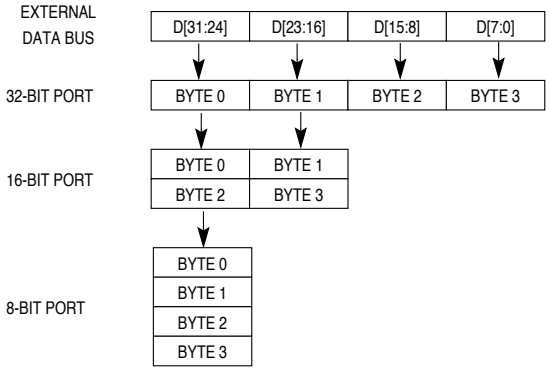

Figure 10-1. MCF5206 Interface to Various Port Sizes

10.3 DRAM CONTROLLER OPERATION

The DRAMC provides a glueless interface to industry-standard DRAMs. The following sections describe the reset operation, definition of DRAM banks, normal mode, Fast Page Mode, burst page mode, Extended Data-Out DRAM support, refresh operation, and alternate master operation.

NOTE

All timing diagrams in the following sections illustrate the fastest possible waveform timing; however, in all cases, the DRAM Controller Timing Register (DCTR) can be programmed to generate slower waveform timing.

10.3.1 Reset Operation

The MCF5206 supports two types of external hardware reset—Master Reset and Normal Reset. Master Reset resets the entire MCF5206 including all functions of the DRAMC. Normal Reset resets all of the functions of the MCF5206 with the exception of the DRAMC Refresh Controller. During Normal Resets, the Refresh Controller continues to generate refresh cycles at the programmed rate and with the programmed cycle timing.

NOTE

Master Reset must be asserted for all power-on resets. Failure to assert Master Reset on power-on reset could result in unpredictable DRAMC behavior.

10.3.1.1 MASTER RESET. During a master reset all registers in the DRAMC are initialized to a known state and all DRAMC operation is halted. The DRAM refresh counter will not count and DRAM refresh cycles will not be generated. Any DRAM transfer or refresh cycle in progress will be immediately terminated.

A master reset is accomplished by asserting and negating the $\overline{\text{RSTI}}$ and $\overline{\text{HIZ}}$ signals simultaneously (see **Section 6.11 Reset Operation**).

NOTE

During a master reset, the DCCR is reset to $000 (giving the slowest refresh rate) and the DCTR is reset to $0000 (giving the fastest waveform timing). After a Master Reset, the user should program the DRAMC Refresh Register (DCRR) and the DRAMC Timing Register (DCTR) such that refresh cycles are generated at the required rate and with the required timing for the DRAM in the system. In general, DRAMs require an initial pause after power-up and require a minimum number of DRAM cycles to be run before the DRAM is ready for use. This “wake-up” sequence must be handled via software.

10.3.1.2 NORMAL RESET. Normal reset is used when the DRAM contains valid data which needs to be maintained through reset. The DRAMC Refresh Register (DCRR), DRAMC Timing Register (DCTR), and the internal DRAMC Refresh controller are unaffected by normal reset. All other MCF5206 registers are reset to the same values during normal resets as during Master Resets. During normal reset, DRAM refreshes will occur at the programmed rate and with the programmed DRAM cycle timing.

A normal reset is accomplished by asserting the $\overline{\text{RSTI}}$ signal while negating the $\overline{\text{HIZ}}$ signal. Resets generated by the internal Software Watchdog Timer are normal resets.

10.3.2 Definition of DRAM Banks

The DRAMC supports as many as two banks of DRAM. You can program each bank independently except for the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ waveform timing (programming the DCTR affects the waveform timing for both banks).

10.3.2.1 BASE ADDRESS AND ADDRESS MASKING. The transfer address generated by the ColdFire core or by an alternate master is compared to the unmasked bits of the base address programmed for each bank in the DRAMC Address Registers (DCAR0 - DCAR1). The bits that are masked is determined by the value programmed in the BAM field in the DRAMC Mask Registers (DCMR0 - DCMR1).

The masking of address bits is used to define the address space of the DRAM bank. Address bits that are masked are not used in the comparison with the transfer address. The base address field (BA31-BA17) in the DCARs and the base address mask field (BAM31-BAM17) in the DCMRs correspond to transfer address bits 31-17. Clearing (unmasking) all bits in the BAM field makes the address space 128 kbyte. For the address space of a DRAM bank to be contiguous, address bits should be masked (BAM bits set to a 1) in ascending order starting with A[17].

For example, if the DCARs and DCMRs are programmed as shown in Table 10-3, DRAM bank 0 would have a 16 Mbyte address space starting at address $04000000, while DRAM bank 1 would have a 1 Mbyte address space starting at address $05000000. A transfer with A[31:24] = $04 will access DRAM bank 0, and a transfer address with A[31:20] = $050 will access DRAM bank 1.

Table 10-3. DRAM Bank Programming Example 1

DRAM BANK	DCAR	DCMR	DRAM ADDRESS SPACE	ADDRESS MATCH
0	$0400	$00FE0000	16 Mbyte	$04xxxxxx
1	$0500	$000E0000	1 Mbyte	$050xxxxx

Refer to **Section 10.4.2.3 DRAM Controller Address Registers (DCAR0 - DCAR1)** and **Section 10.4.2.4 DRAM Controller Mask Register (DCMR0 - DCMR1)** for further details.

NOTE

The ColdFire core outputs 32 bits of address to the internal bus controller. Of these 32 bits, only A[27:0] are output to pins on the MCF5206. The output of A[27:24] are dependent on the setting of PAR3-PAR0 in the Pin Assignment Register (PAR) in the SIM.

NOTE

The MCF5206 compares the address for the current bus transfer with the address and mask bits in the Chip-Select Address Registers (CSARs), DRAM Controller Address Registers (DCARs) and the Chip-Select Mask Register

(CSMRs) and DRAM Controller Mask Register (DCMRs), looking for a match.

The priority is listed in Table 10-4 (from highest priority to lowest priority): Address Registers (CSARs), DRAM

Table 10-4. Chip-Select, DRAM and Default Memory Address Decoding Priority

Chip-select 0	Highest
Chip-select 1	
Chip-select 2	
Chip-select 3	
Chip-select 4	
Chip-select 5	
Chip-select 6	
Chip-select 7	
Dram Bank 0	
Dram Bank 1	
Default Memory	Lowest

The MCF5206 will compare the address and mask in Chip-select 0 - 7 (Chip-select 0 is compared first), then the address and mask in DRAM 0 - 1. If the address does not match in either or these, the MCF5206 will use the control bits in the Default Memory Control Register (DMCR) to control the bus transfer. If the Default Memory Control Register (DMCR) control bits are used, no chip-select or DRAM control signals will be asserted during the transfer.

10.3.2.2 ACCESS PERMISSION. DRAM bank accesses can be restricted based on transfer direction and attributes. Each DRAM bank can be enabled for read and/or write transfers using the WR and RD bits in the DCCRs. Each DRAM bank can have supervisor data, supervisor code, user data, and user code transfers masked from their address space using the SD, SC, UD, and UC bits in the DCMRs. The transfer address must match, the transfer direction must be enabled, and transfer attributes must be unmasked for a transfer to a DRAM bank to occur.

For example, if the DCARs, DCMRs, and DCCRs are programmed as shown in Table 10-5, DRAM bank 0 would start at address $04000000, and be 16 Mbyte, read/write, and available for supervisor transfers only. DRAM bank 1 would start at address $05000000 and be 1Mbyte, read-only, and available to all address spaces.

If a user data -read transfer was attempted to address $04000000, the transfer would not access DRAM bank 0, since user space transfers are masked. The transfer would not access DRAM bank 1 since the addresses do not match. Therefore, a Default Memory transfer would occur.

If a user data write transfer was attempted to address $05000000, the transfer would not access DRAM bank 0 since the addresses do not match. The transfer would not access

DRAM bank 1 since this bank is not enabled for writes. Therefore, a Default Memory transfer would occur.

Table 10-5. DRAM Bank Programming Example 2

DRAM BANK	DCAR	DCMR	DCCR	ADDRESS MATCH	TRANSFER TYPE	READ/WRITE
0	$0400	$00FE0006	$03	$04xxxxxx	supervisor-only	read/write
1	$0500	$000E0000	$01	$050xxxxx	all transfer types	read-only

Refer to **Section 10.4.2.4 DRAM Controller Mask Register (DCMR0 - DCMR1)** and **Section 10.4.2.5 DRAM Controller Control Register (DCCR0 - DCCR1)** for further details.

10.3.2.3 TIMING. The timing of $\overline{RAS}$ and $\overline{CAS}$ assertion and negation can be customized to meet the timing specifications for the specific DRAM being used. This programmed waveform timing is used for both banks.

Refer to **Section 10.4.2.2 DRAM Controller Timing Register (DCTR)** for further details.

10.3.2.4 PAGE MODE. Each bank can be configured for normal mode, fast page mode, or burst page mode. Normal mode DRAM cycles supply a row address and a column address for each transfer. Fast page mode DRAM cycles supply a row address and a column address for the first transfer to a page and only a column address on successive transfers to that page. Burst page mode is a combination of normal mode and fast page mode. For transfers where the port size is larger or the same as the operand size (non-burst transfers), burst page mode operates the same as normal mode. For transfers where the operand size is larger than the port size (burst transfers), burst page mode operates the same as fast page mode.

Refer to **10.3.3 Normal Mode Operation**, **10.3.4 Fast Page Mode Operation**, **10.3.5 Burst Page-Mode Operation**, and **Section 10.4.2.5 DRAM Controller Control Register (DCCR0 - DCCR1)** for further details.

10.3.2.5 PORT SIZE/PAGE SIZE. Each DRAM bank can be programmed for 8-, 16-, or 32-bit port sizes. Each bank can also have an internal bank page size of 512 byte, 1 kbyte, or 2 kbyte.

Refer to **Section 10.4.2.5 DRAM Controller Control Register (DCCR0 - DCCR1)** for further details.

10.3.2.6 ADDRESS MULTIPLEXING. The MCF5206 provides internal address multiplexing of the row address and column address for DRAM transfers. The internal address multiplexing is used for all ColdFire core initiated DRAM transfers and can selectively be used for alternate master initiated DRAM transfers. No external logic is required in the system to handle DRAM address multiplexing when the internal multiplexing is used. In addition, the multiplexing scheme allows a single printed circuit board layout to support multiple DRAM memory sizes (allowing for easy memory upgrades).

A subset of the address pins will be connected directly to the address inputs of the DRAM to supply the row address and column address. The DRAM port size and bank page size determine which address pins should be connected to the address inputs of the DRAM. In Figure 10-2, the address multiplexing scheme is illustrated for an 8-bit DRAM with 9 address inputs using a 512 byte page size (PS=01 and BPS=00 in the DCCR). In this case, the DRAM address inputs (DA[x]) would be connected to the MCF5206 address pins (A[x]) in the following order: A[9] to DA[0], A[10] to DA[1], A[11] to DA[2], A[12] to DA[3], A[13] to DA[4], A[14] to DA[5], A[15] to DA[6], A[16] to DA[7], and A[17] to DA[8]. When the ColdFire core initiates a transfer to an address location in the DRAM, the MCF5206 will drive the internal transfer address IA[27:0] onto the MCF5206 address pins A[27:0] and will assert $\overline{RAS}$. This will strobe the internal transfer address bits IA[17:9] into the DRAM as the row address. Then the MCF5206 will internally multiplex and drive the internal transfer address bits IA[8:0] onto the MCF5206 address pins A[17:9] and will assert $\overline{CAS}$. This will strobe the internal transfer address bits IA[8:0] into the DRAM as the column address.

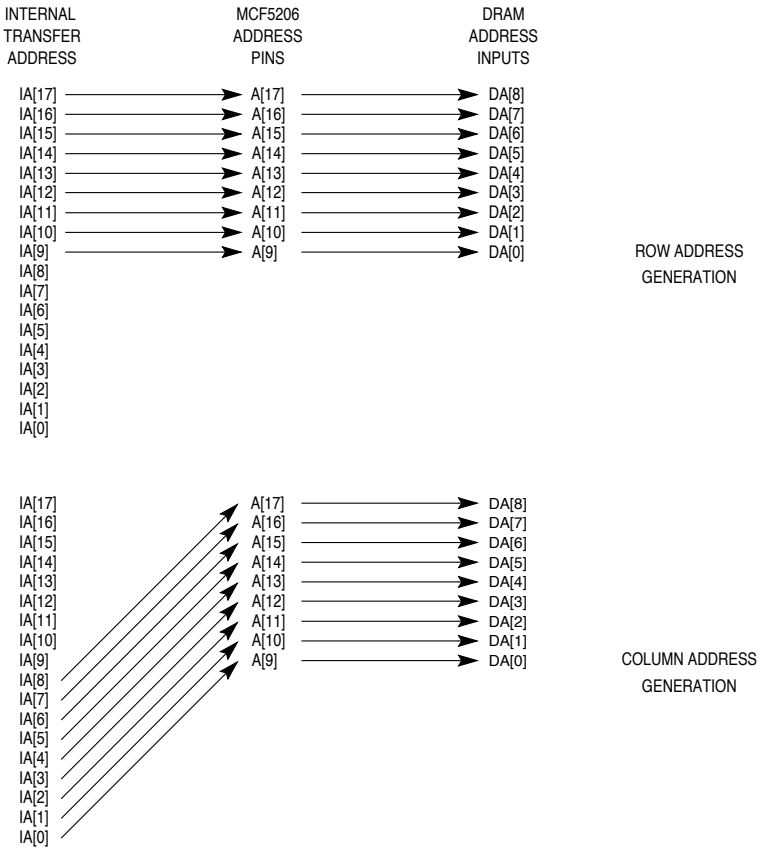

Figure 10-2. Address Multiplexing For 8-bit DRAM With 512 byte Page Size

The port size (PS) and the bank page size (BPS) determine which address bus pins are used to drive the row address and column address. Table 10-6, Table 10-7, and Table 10-8 show which internal transfer address bits are driven on each address pin during the assertion of $\overline{RAS}$ and during the assertion of $\overline{CAS}$ for all combinations of port size (PS) and bank page size (BPS). The shaded address pins in each PS/BPS configuration will output the row address during the assertion of $\overline{RAS}$ and the column address during the assertion of $\overline{CAS}$. These signals should be connected to the DRAM address inputs. The number of address signals used depends on the size of the DRAM. Because byte $\overline{CAS}$ signals ($\overline{CAS}$[3:0]) are provided, A[0] is unnecessary for 16-bit DRAMs and A[1:0] are unnecessary for 32-bit DRAMs.

Table 10-6. 8-bit Port Size Address Multiplexing Configurations

MCF5206 ADDRESS PIN	PS = 8-BIT BPS = 512 BYTE		MCF5206 ADDRESS PIN	PS = 8-BIT BPS = 1 KBYTE		MCF5206 ADDRESS PIN	PS = 8-BIT BPS = 2 KBYTE	
	ROW ADDRESS	COLUMN ADDRESS		ROW ADDRESS	COLUMN ADDRESS		ROW ADDRESS	COLUMN ADDRESS
A[27]	IA[27]	IA[26]	A[27]	IA[27]	IA[26]	A[27]	IA[27]	IA[26]
A[26]	IA[26]	IA[26]	A[26]	IA[26]	IA[26]	A[26]	IA[26]	IA[26]
A[25]	IA[25]	IA[24]	A[25]	IA[25]	IA[24]	A[25]	IA[25]	IA[24]
A[24]	IA[24]	IA[24]	A[24]	IA[24]	IA[24]	A[24]	IA[24]	IA[24]
A[23]	IA[23]	IA[22]	A[23]	IA[23]	IA[22]	A[23]	IA[23]	IA[22]
A[22]	IA[22]	IA[22]	A[22]	IA[22]	IA[22]	A[22]	IA[22]	IA[22]
A[21]	IA[21]	IA[20]	A[21]	IA[21]	IA[20]	A[21]	IA[21]	IA[10]
A[20]	IA[20]	IA[20]	A[20]	IA[20]	IA[20]	A[20]	IA[20]	IA[9]
A[19]	IA[19]	IA[18]	A[19]	IA[19]	IA[9]	A[19]	IA[19]	IA[8]
A[18]	IA[18]	IA[18]	A[18]	IA[18]	IA[8]	A[18]	IA[18]	IA[7]
A[17]	IA[17]	IA[8]	A[17]	IA[17]	IA[7]	A[17]	IA[17]	IA[6]
A[16]	IA[16]	IA[7]	A[16]	IA[16]	IA[6]	A[16]	IA[16]	IA[5]
A[15]	IA[15]	IA[6]	A[15]	IA[15]	IA[5]	A[15]	IA[15]	IA[4]
A[14]	IA[14]	IA[5]	A[14]	IA[14]	IA[4]	A[14]	IA[14]	IA[3]
A[13]	IA[13]	IA[4]	A[13]	IA[13]	IA[3]	A[13]	IA[13]	IA[2]
A[12]	IA[12]	IA[3]	A[12]	IA[12]	IA[2]	A[12]	IA[12]	IA[1]
A[11]	IA[11]	IA[2]	A[11]	IA[11]	IA[1]	A[11]	IA[11]	IA[0]
A[10]	IA[10]	IA[1]	A[10]	IA[10]	IA[0]	A[10]	IA[10]	IA[10]
A[9]	IA[9]	IA[0]	A[9]	IA[9]	IA[9]	A[9]	IA[9]	IA[9]

Table 10-7. 16-bit Port Size Address Multiplexing Configurations

MCF5206 ADDRESS PIN	PS = 16-BIT BPS = 512 BYTE		MCF5206 ADDRESS PIN	PS = 16-BIT BPS = 1 KBYTE		MCF5206 ADDRESS PIN	PS = 16-BIT BPS = 2 KBYTE	
	ROW ADDRESS	COLUMN ADDRESS		ROW ADDRESS	COLUMN ADDRESS		ROW ADDRESS	COLUMN ADDRESS
A[27]	IA[27]	IA[27]	A[27]	IA[27]	IA[27]	A[27]	IA[27]	IA[27]
A[26]	IA[26]	IA[25]	A[26]	IA[26]	IA[25]	A[26]	IA[26]	IA[25]
A[25]	IA[25]	IA[25]	A[25]	IA[25]	IA[25]	A[25]	IA[25]	IA[25]
A[24]	IA[24]	IA[23]	A[24]	IA[24]	IA[23]	A[24]	IA[24]	IA[23]
A[23]	IA[23]	IA[23]	A[23]	IA[23]	IA[23]	A[23]	IA[23]	IA[23]
A[22]	IA[22]	IA[21]	A[22]	IA[22]	IA[21]	A[22]	IA[22]	IA[21]
A[21]	IA[21]	IA[21]	A[21]	IA[21]	IA[21]	A[21]	IA[21]	IA[21]
A[20]	IA[20]	IA[19]	A[20]	IA[20]	IA[19]	A[20]	IA[20]	IA[10]
A[19]	IA[19]	IA[19]	A[19]	IA[19]	IA[19]	A[19]	IA[19]	IA[9]
A[18]	IA[18]	IA[17]	A[18]	IA[18]	IA[9]	A[18]	IA[18]	IA[8]
A[17]	IA[17]	IA[17]	A[17]	IA[17]	IA[8]	A[17]	IA[17]	IA[7]
A[16]	IA[16]	IA[8]	A[16]	IA[16]	IA[7]	A[16]	IA[16]	IA[6]
A[15]	IA[15]	IA[7]	A[15]	IA[15]	IA[6]	A[15]	IA[15]	IA[5]
A[14]	IA[14]	IA[6]	A[14]	IA[14]	IA[5]	A[14]	IA[14]	IA[4]
A[13]	IA[13]	IA[5]	A[13]	IA[13]	IA[4]	A[13]	IA[13]	IA[3]
A[12]	IA[12]	IA[4]	A[12]	IA[12]	IA[3]	A[12]	IA[12]	IA[2]
A[11]	IA[11]	IA[3]	A[11]	IA[11]	IA[2]	A[11]	IA[11]	IA[1]
A[10]	IA[10]	IA[2]	A[10]	IA[10]	IA[1]	A[10]	IA[10]	IA[10]
A[9]	IA[9]	IA[1]	A[9]	IA[9]	IA[9]	A[9]	IA[9]	IA[9]

Table 10-8. 32-bit Port Size Address Multiplexing Configurations

MCF5206 ADDRESS PIN	PS = 32-BIT BPS = 512 BYTE		MCF5206 ADDRESS PIN	PS = 32-BIT BPS = 1 KBYTE		MCF5206 ADDRESS PIN	PS = 32-BIT BPS = 2 KBYTE	
	ROW ADDRESS	CAS		ROW ADDRESS	CAS		ROW ADDRESS	CAS
A[27]	IA[27]	IA[26]	A[27]	IA[27]	IA[26]	A[27]	IA[27]	IA[26]
A[26]	IA[26]	IA[26]	A[26]	IA[26]	IA[26]	A[26]	IA[26]	IA[26]
A[25]	IA[25]	IA[24]	A[25]	IA[25]	IA[24]	A[25]	IA[25]	IA[24]
A[24]	IA[24]	IA[24]	A[24]	IA[24]	IA[24]	A[24]	IA[24]	IA[24]
A[23]	IA[23]	IA[22]	A[23]	IA[23]	IA[22]	A[23]	IA[23]	IA[22]
A[22]	IA[22]	IA[22]	A[22]	IA[22]	IA[22]	A[22]	IA[22]	IA[22]
A[21]	IA[21]	IA[20]	A[21]	IA[21]	IA[20]	A[21]	IA[21]	IA[20]
A[20]	IA[20]	IA[20]	A[20]	IA[20]	IA[20]	A[20]	IA[20]	IA[20]
A[19]	IA[19]	IA[18]	A[19]	IA[19]	IA[18]	A[19]	IA[19]	IA[10]
A[18]	IA[18]	IA[18]	A[18]	IA[18]	IA[18]	A[18]	IA[18]	IA[9]
A[17]	IA[17]	IA[16]	A[17]	IA[17]	IA[9]	A[17]	IA[17]	IA[8]
A[16]	IA[16]	IA[16]	A[16]	IA[16]	IA[8]	A[16]	IA[16]	IA[7]
A[15]	IA[15]	IA[8]	A[15]	IA[15]	IA[7]	A[15]	IA[15]	IA[6]
A[14]	IA[14]	IA[7]	A[14]	IA[14]	IA[6]	A[14]	IA[14]	IA[5]
A[13]	IA[13]	IA[6]	A[13]	IA[13]	IA[5]	A[13]	IA[13]	IA[4]
A[12]	IA[12]	IA[5]	A[12]	IA[12]	IA[4]	A[12]	IA[12]	IA[3]
A[11]	IA[11]	IA[4]	A[11]	IA[11]	IA[3]	A[11]	IA[11]	IA[2]
A[10]	IA[10]	IA[3]	A[10]	IA[10]	IA[2]	A[10]	IA[10]	IA[10]
A[9]	IA[9]	IA[2]	A[9]	IA[9]	IA[9]	A[9]	IA[9]	IA[9]

The BPS field in each DCCR defines the DRAMC internal page size. The internal page size is used by the DRAMC to determine whether an transfer is a page hit or a page miss. The page size of the DRAM used in the bank will not always be the same as the DRAMC internal page size. For example, if a 2 kbyte page size is selected and an 8-bit wide DRAM is used, 11 address bits and 1 $\overline{\text{CAS}}$ signal are needed to define the page. However, if a 2 kbyte page size is selected and a 32-bit wide DRAM is used, only 9 address signals and 4 $\overline{\text{CAS}}$ signals are needed to define the page. Using a DRAM which has a larger page size than is listed in the actual DRAM page size column of Table 10-9 for a given internal page size and port size will give no performance advantage.

To allow for future upgrades to larger DRAMs without requiring multiple printed circuit board layouts, the page size must remain constant. After the page size has been selected, use the tables to determine which address pins to use for the maximum DRAM size. These traces can then be routed to the DRAM socket on the printed circuit board.

Table 10-9. Bank Page Size Versus Actual DRAM Page Size

BANK PAGE SIZE (BPS)	PORT SIZE	PAGE ADDRESS	ACTUAL DRAM PAGE SIZE
512 byte	8-bit	A[8:0]	512 byte
	16-bit	A[8:1]	256 byte
	32-bit	A[8:2]	128 byte
1 kbyte	8-bit	A[9:0]	1 kbyte
	16-bit	A[9:1]	512 byte
	32-bit	A[9:2]	256 byte
2 kbyte	8-bit	A[10:0]	2 kbyte
	16-bit	A[10:1]	1kbyte
	32-bit	A[10:2]	512 byte

From a hardware point of view, a smaller DRAM will simply not connect to the upper address pins. When a larger DRAM is installed, all address pins will be connected. From a software point of view, the DRAMC Mask Register (DCMR) contents will be modified to mask more of the address bits for the larger DRAM. The bank page size (BPS) in the DRAMC Control Register (DCCR) must remain the same, even if the larger DRAM (upgraded to) can support a larger page size. If the BPS field is changed, the address multiplexing will also change—requiring a different printed circuit board layout.

As an example, suppose the system DRAM is 8-bits wide and can range from 1Mbyte (1 M x 8-bit) to 4 Mbyte (4 M x 8-bit), with a page size of 1 kbyte. Referring to Table 10-8, address pins A[10:19] and A[21] should be routed to the DRAM socket pins. For the 4 M x 8 DRAM, the MCF5206 address pins A[10:19] and A[21] will be connected to the DRAM address inputs A[0:10] (see Figure 10-3). For the 1 M x 8 DRAM, the MCF5206 address pins A[10:19] will be connected to the DRAM address inputs A[0:9] (see Figure 10-4). Because the address connections for the 1 M x 8 are a subset of those for the 4 M x 8, the address multiplexing scheme allows a system using the MCF5206 to upgrade the memory size without requiring different printed circuit board layouts. The only thing that must be changed is the number of bits masked in the DCMR.

It should be noted that the page size, in this example, is determined by the 1 M x 8 DRAM (9 column address bits gives a page size of 1 kbyte), and that even though the 4 M x 8 DRAM could support a 2 kbyte page size, the page size must be programmed to 1 kbyte to keep the address multiplexing the same.

For the 4 M x 8 DRAM, the DCCR and DCMR would be programmed as follows:

DCCR: $57 (port size = 8-bit, page size = 1kbyte, burst page mode, read/write)
DCMR: $001e0000 (A[20:17] are masked => 4 Mbyte)

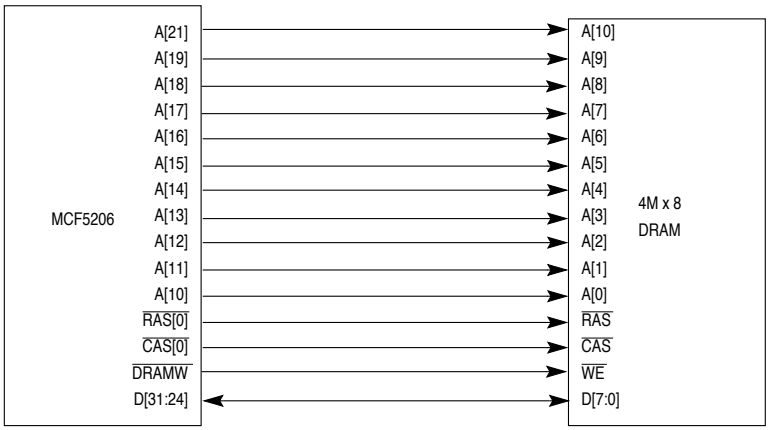

Figure 10-3. Connection Diagram for 4Mbyte DRAM with 8-bit Port and 1Kbyte Page

For the 1 M x 8 DRAM, the DCCR and DCMR would be programmed as follows:

DCCR: $57 (port size = 8-bit, page size = 1kbyte, burst page mode, read/write)
DCMR: $000e0000 (A[19:17] are masked => 1 Mbyte).

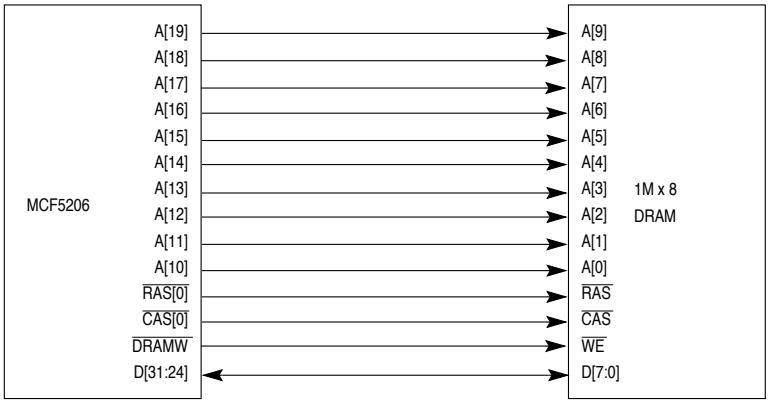

Figure 10-4. Connection Diagram for 1Mbyte DRAM with 8-Bit Port and 1Kbyte Page

10.3.3 Normal Mode Operation

Normal mode is the simplest form of DRAM transfer. In this mode, row addresses and column addresses are supplied for every transfer. For DRAM transfers initiated by the ColdFire core that access a bank programmed for normal mode, the MCF5206 supplies a row address on the address bus, drives $\overline{\text{DRAMW}}$ to indicate whether a read or a write

is occurring and asserts $\overline{\text{RAS}}$. The MCF5206 then drives the column address onto the same address pins and asserts $\overline{\text{CAS}}$. When the cycle is complete, both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are negated.

10.3.3.1 NONBURST TRANSFER IN NORMAL MODE. A nonburst transfer to DRAM will occur when the operand size is the same or smaller than the DRAM port size (e.g.,longword transfer to a 32-bit port, or byte transfer to a 16-bit port). Nonburst transfers always start with the assertion of $\overline{\text{TS}}$.

The start of a transfer to a DRAM bank can be delayed by the DRAMC until the programmed $\overline{\text{RAS}}$ precharge time is met. A transfer to a different DRAM bank than the previous transfer will never be delayed due to $\overline{\text{RAS}}$ precharge since that bank will have already been precharged.

The timing of nonburst reads and nonburst writes is identical in normal page mode, with the exception of when the DRAM drives data on reads and when the MCF5206 drives data on writes.

The fastest possible nonburst transfer in normal mode requires 3 clocks with a 1.5 clock $\overline{\text{RAS}}$ precharge time. You can program the DCTR to generate slower normal mode transfers.

Figure 10-6 shows the timing of a back-to-back nonburst byte-read transfer to an 8-bit port in normal mode.

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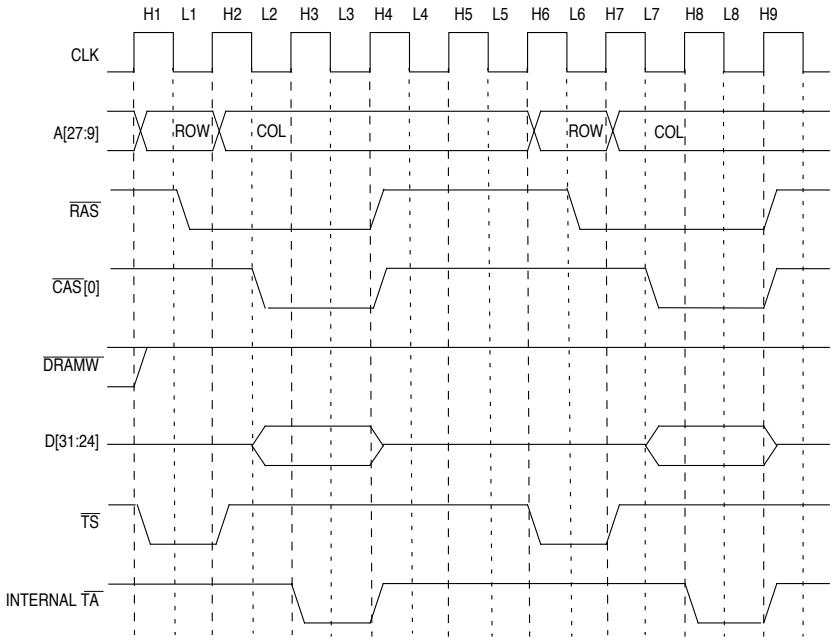

Figure 10-5. Byte Read Transfers in Normal Mode with 8-bit DRAM

Clock H1

The first DRAM-read transfer starts in H1. During H1, the MCF5206 drives the row address on the A[27:9], drives $\overline{\text{DRAMW}}$ high indicating a DRAM-read transfer, drives SIZ[1:0] to $1 indicating a byte transfer, and asserts $\overline{\text{TS}}$.

Clock L1

The MCF5206 asserts $\overline{\text{RAS}}$ to indicate the row address is valid on the address bus.

Clock H2

The MCF5206 negates $\overline{\text{TS}}$, and drives the column address on the address bus.

Clock L2

The MCF5206 asserts $\overline{\text{CAS}}$[0] to indicate the column address is valid on the address bus. At this point, the DRAM will turn on its output drivers and begin driving data on D[31:24].

Clock H3

The internal transfer acknowledge asserts to indicate that the current transfer will be completed and the data on the D[31:24] will be registered on the next rising edge of CLK.

Clock H4

The MCF5206 registers the read data driven by the DRAM and negates the internal transfer acknowledge, $\overline{RAS}$ and $\overline{CAS}$[0], ending the first byte-read transfer. This begins the $\overline{RAS}$ precharge. Once $\overline{CAS}$[0] is negated the DRAM disables its output drivers, and the data bus is three-stated.

Clock H6

Clock H6 is the earliest the next transfer initiated by the ColdFire core can start. The second DRAM byte-read transfer starts in H6. During H6, the MCF5206 drives the row address on the A[27:9], drives $\overline{DRAMW}$ high indicating a DRAM-read transfer, drives SIZ[1:0] to $1 indicating a byte transfer, and asserts $\overline{TS}$.

Clock L6

Clock L6 is the same as Clock L1.

Clock H7

Clock H7 is the same as Clock H2.

Clock L7

Clock L7 is the same as Clock L2.

Clock H8

Clock H8 is the same as Clock H3.

Clock H9

Clock H9 is the same as Clock H4.

10.3.3.2 BURST TRANSFER IN NORMAL MODE. A burst transfer to DRAM will be generated when the operand size is larger than the DRAM bank port size (e.g., line transfer to a 32-bit port, longword transfer to an 8-bit port). On all DRAM transfers, the MCF5206 asserts $\overline{TS}$ only once. The start of the secondary transfers of a burst is delayed by the DRAMC until the programmed $\overline{RAS}$ precharge time is reached.

The timing of burst reads and burst writes is identical in normal page mode, with the exception of when the DRAM drives data on reads and when the MCF5206 drives data on writes.

The fastest possible burst transfer in normal mode requires 3 clocks for the first transfer of the burst and 4 clocks for the secondary transfers (including a 1.5 clock $\overline{RAS}$ precharge time). You can program the DCTR to generate slower normal mode transfers.

Figure 10-6 shows the timing of a burst longword write transfer to a 16-bit port in normal mode.

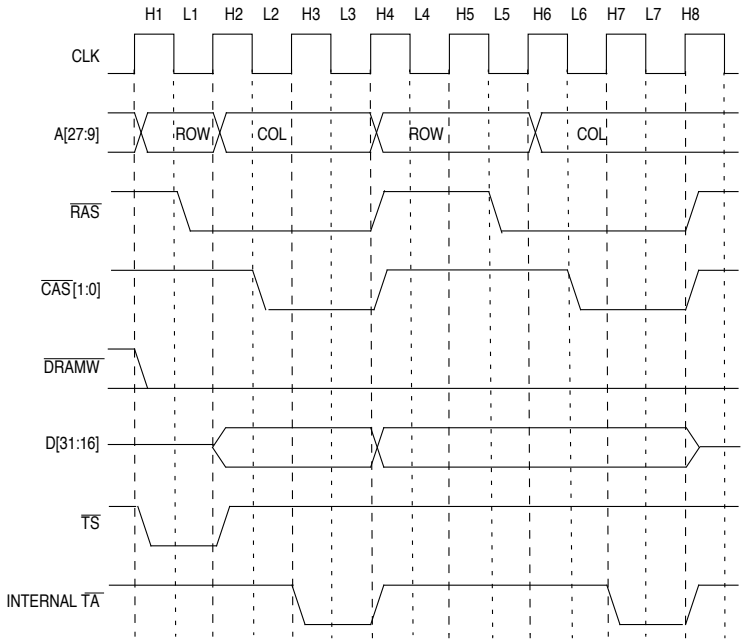

Figure 10-6. Longword Write Transfer in Normal Mode with 16-bit DRAM

Clock H1

The first DRAM write transfer of the burst starts in H1. During H1, the MCF5206 drives the row address on A[27:9], drives $\overline{\text{DRAMW}}$ low indicating a DRAM write transfer, drives SIZ[1:0] to $0 indicating a longword transfer, and asserts $\overline{\text{TS}}$. The address driven on the A[27:9] corresponds to the DRAM row address for the first transfer of the burst.

Clock L1

The MCF5206 asserts $\overline{\text{RAS}}$ to indicate the row address is valid on A[27:9].

Clock H2

The MCF5206 negates $\overline{\text{TS}}$, drives the column address on A[27:9], and begins driving the data on D[31:16] for the first word write of the longword burst.

Clock L2

The MCF5206 asserts $\overline{\text{CAS}}$[1:0] to indicate the column address is valid on the A[27:9].

Clock H3

The internal transfer acknowledge asserts to indicate the first word transfer of the longword burst will be completed on the next rising edge of CLK.

Clock H4

The MCF5206 negates the internal transfer acknowledge, $\overline{RAS}$ and $\overline{CAS}$[1:0], ending the first word write transfer of the longword burst. This begins the $\overline{RAS}$ precharge. The MCF5206 drives the row address on A[27:9], and begins driving the data on D[31:16] for the second word write of the longword burst.

Clock L4/H5

The MCF5206 continues to negate $\overline{RAS}$ to meet the precharge time.

Clock L5

After the $\overline{RAS}$ precharge time is reached, the MCF5206 asserts $\overline{RAS}$ to indicate the row address is valid on A[27:9].

Clock H6

The MCF5206 drives the column address on A[27:9].

Clock L6

The MCF5206 asserts $\overline{CAS}$[1:0] to indicate the column address is valid on A[27:9].

Clock H7

Clock H7 is the same as Clock H3.

Clock H8

The MCF5206 negates the internal transfer acknowledge, $\overline{RAS}$ and $\overline{CAS}$[1:0], ending the second word write transfer of the longword burst. This begins the $\overline{RAS}$ precharge. When the burst write is completed, D[31:0] is three-stated.

10.3.4 Fast Page Mode Operation

Fast page mode operation allows faster successive transfers to locations in DRAM that have the same row address. All locations with the same row address are said to be on the same “page.” Successive transfers that have the same row address as the initial transfer are called “page hits,” while successive transfers with different row addresses are called “page misses.”

On the initial transfer to a page, the DRAMC stores the row address. The address of a successive transfer is compared with the stored row address to determine if the transfer

is a page hit or a page miss. For a page size of 512 byte (BPS=$0 in the DCTR), bits 31-9 of the transfer address must match the corresponding bits stored as the active row address to be a page hit. For a page size of 1 kbyte (BPS=$1), bits 31-10 of the transfer address must match the corresponding bits of the active row address to be a page hit. For a page size of 2 kbyte (BPS=$2), bits 31-11 of the transfer address must match the corresponding bits of the active row address to be a page hit.

Fast page-mode transfers are facilitated by having the $\overline{RAS}$ signal remain asserted while asserting $\overline{CAS}$ to access successive column locations determined by the column address. Once $\overline{RAS}$ asserts on a transfer to a page, the page is said to be “open” and $\overline{RAS}$ will remain asserted on all successive transfers to that page. If a transfer to a location in the current DRAM bank is a page hit, only the column address will be driven and $\overline{CAS}$ will be asserted.

In fast page mode, $\overline{RAS}$ will negate (precharge), “closing” the current page, under the following conditions:

1. A transfer occurs to an address in the current DRAM bank that is a page miss
2. A transfer occurs to an address in the other DRAM bank
3. The MCF5206 loses bus mastership
4. A refresh cycle is pending

In each of these cases, the $\overline{RAS}$ will negate and the DRAMC will not allow an access to that bank until the $\overline{RAS}$ precharge time is met.

10.3.4.1 BURST TRANSFER IN FAST PAGE MODE. A burst transfer to DRAM will be generated when the operand size is larger than the DRAM bank port size (e.g., line transfer to a 32-bit port, longword transfer to an 8-bit port). Burst transfers can access from two to 16 segments of data in a single transfer. On all DRAM transfers the MCF5206 asserts $\overline{TS}$ only once. The internal $\overline{TA}$ is asserted to indicate the transfer of each segment of data. The start of the secondary transfers of a burst will be delayed by the DRAMC until the programmed $\overline{RAS}$ precharge time is reached.

The timing of burst reads and burst writes is identical in fast page mode, with the exception of when the DRAM drives data on reads and when the MCF5206 drives data on writes.

The fastest possible burst transfer in normal mode takes 3 clocks for the initial transfer, 2 clocks for secondary transfers with a 0.5 clock $\overline{CAS}$ precharge time and a 1.5 clock $\overline{RAS}$ precharge time. You can program the DCTR to generate slower fast page mode transfers.

Figure 10-7 shows the timing of a word write transfer to an 8-bit port in fast page mode.

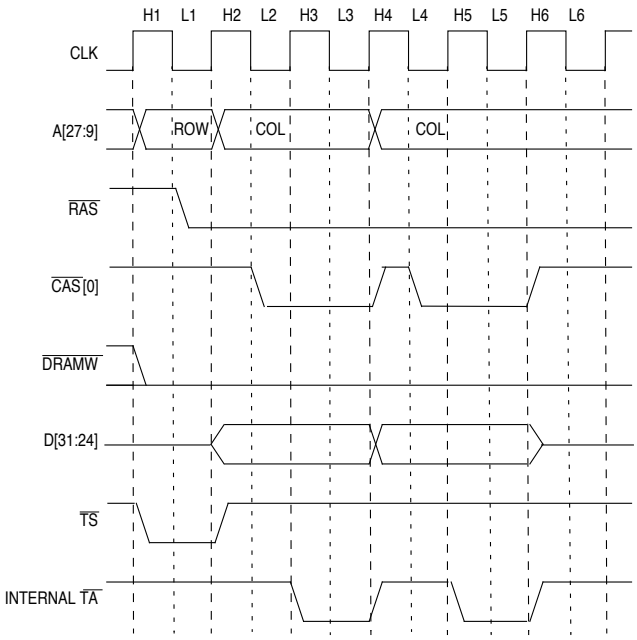

Figure 10-7. Word Write Transfer in Fast Page Mode with 8-Bit DRAM

Clock H1

The first byte write transfer of the word burst starts in H1. During H1, the MCF5206 drives the row address on A[27:9], drives DRAMW low indicating a DRAM write transfer, drives SIZ[1:0] to $2 indicating a word transfer, and asserts TS. The address driven on A[27:9] corresponds to the row address for the first byte transfer of the burst.

Clock L1

The MCF5206 asserts RAS to indicate the row address is valid on A[27:9].

Clock H2

The MCF5206 negates TS, drives the column address on A[27:9], and begins driving the data on D[31:24].

Clock L2

The MCF5206 asserts CAS[0] to indicate the column address is valid on A[27:9].

Clock H3

The internal transfer acknowledge asserts to indicate that the first byte transfer of the word burst will be completed on the next rising edge of CLK.

Clock H4

The MCF5206 negates the internal transfer acknowledge, and $\overline{CAS}$[0] ending the first byte write transfer of the word burst. At this point, the new page has been opened; therefore, the MCF5206 continues to assert $\overline{RAS}$. The negation of $\overline{CAS}$[0] begins the $\overline{CAS}$ precharge. The MCF5206 drives the next column address on A[27:9] and the next data is driven on D[31:24].

Clock L4

Clock L4 is the same as Clock L2.

Clock H5

Clock H5 is the same as Clock H3.

Clock H6

The MCF5206 negates the internal transfer acknowledge, and $\overline{CAS}$[0] ending the final byte write of the word burst. Because the bank is in fast page mode, MCF5206 continues to assert $\overline{RAS}$. The negation of $\overline{CAS}$[0] begins the $\overline{CAS}$ precharge. When the burst write is completed, the MCF5206 three-states D[31:0].

10.3.4.2 PAGE HIT READ TRANSFER IN FAST PAGE MODE.

A read transfer to an open page results in a page-hit read. The timing of page-hit reads differs from the timing of page-hit writes (page-hit writes are described in **Section 10.3.4.3 Page-Hit Write Transfer in Fast Page Mode**). The start of a page-hit read transfer to a DRAM bank in fast page mode can be delayed by the DRAMC until the programmed $\overline{CAS}$ precharge time is reached.

The fastest possible nonburst page-hit read transfer in fast page mode takes 2 clocks with a 0.5 clock $\overline{CAS}$ precharge time. The fastest possible burst page-hit read transfer in fast page mode takes 2 clocks for the initial transfer, and 2 clocks for all secondary reads with a 0.5 clock CAS precharge time. You can program the DCTR to generate slower fast page mode transfers.

Figure 10-8 shows the timing of a nonburst read opening a page and a subsequent page-hit read being generated. The first transfer that opens the page is a longword read transfer from a 32-bit port in fast page mode. The first read transfer is followed by a second page-hit longword read transfer. The timing of a page-hit read transfer is the same regardless of whether the page was opened by a burst read, burst write, nonburst read, or nonburst write transfer.

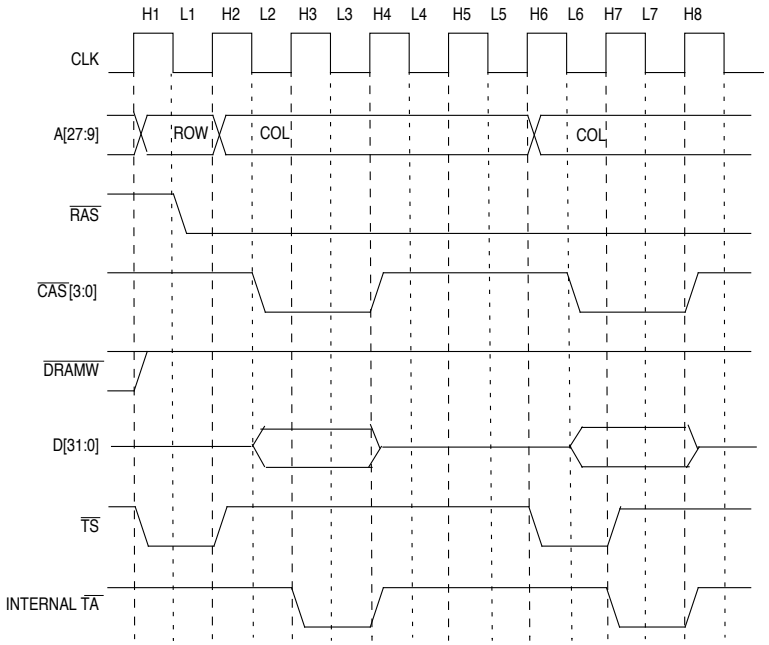

Figure 10-8. Longword Read Transfer Followed by a Page Hit Longword Read Transfer in Fast Page Mode with 32-Bit DRAM

Clock H1

The longword read transfer starts in H1. During H1, the MCF5206 drives the row address on A[27:9], drives $\overline{\text{DRAMW}}$ high indicating a DRAM read transfer, drives SIZ[1:0] to $0 indicating a longword transfer, and asserts $\overline{\text{TS}}$.

Clock L1

The MCF5206 asserts $\overline{\text{RAS}}$ to indicate the row address is valid on A[27:9].

Clock H2

The MCF5206 negates $\overline{\text{TS}}$, and drives the column address on A[27:9].

Clock L2

The MCF5206 asserts $\overline{\text{CAS}}$[3:0] to indicate the column address is valid on A[27:9]. At this point the DRAM will turn on its output drivers and begin driving data on D[31:0].

Clock H3

The internal transfer acknowledge asserts to indicate that the longword read transfer will be completed and that data on D[31:0] will be registered on the next rising edge of CLK.

Clock H4

The MCF5206 negates the internal transfer acknowledge, and $\overline{CAS}$[3:0], ending the longword read transfer. At this point the new page has been opened; therefore, the MCF5206 continues to assert $\overline{RAS}$. Once $\overline{CAS}$[3:0] are negated the DRAM disables its output drivers and the D[31:0] are three-stated. The negation of $\overline{CAS}$[3:0] begins the $\overline{CAS}$ precharge.

Clock H6

Clock H6 is the earliest the next transfer initiated by the ColdFire core can start. In this case, a page-hit longword read is shown. The page-hit longword read transfer starts in H6. During H6, the MCF5206 drives the column address on A[27:9], drives $\overline{DRAMW}$ high indicating a DRAM read transfer, drives SIZ[1:0] to $0 indicating a longword transfer, and asserts $\overline{TS}$.

Clock L6

The MCF5206 asserts $\overline{CAS}$[3:0] to indicate the column address is valid on A[27:9]. At this point, the DRAM will turn on its output drivers and begin driving data on D[31:0].

Clock H7

Clock H7 is the same as Clock H3.

Clock H8

The MCF5206 negates the internal transfer acknowledge, and $\overline{CAS}$[3:0], ending the page-hit longword read transfer. Since the DRAM bank is in Fast Page Mode, the MCF5206 continues to assert $\overline{RAS}$. Once $\overline{CAS}$[3:0] are negated the DRAM disables it's output drivers and D[31:0] are three-stated. The negation of $\overline{CAS}$[3:0] begins the $\overline{CAS}$ precharge.

10.3.4.3 PAGE-HIT WRITE TRANSFER IN FAST PAGE MODE. A write transfer to an open page results in a page-hit write. The timing of page-hit write transfers differs from the timing of page-hit read transfers. On a page-hit write transfer, $\overline{CAS}$ is asserted one cycle later than in a page-hit read transfer. This is because the write data is not driven until the cycle after $\overline{TS}$ is asserted and data must be set up prior to $\overline{CAS}$ assertion. The start of a page-hit write transfer to a DRAM bank in fast page mode can be delayed by the DRAMC until the programmed $\overline{CAS}$ precharge time is reached.

The fastest possible nonburst page-hit write transfer in fast page mode requires 3 clocks. The fastest possible burst page-hit write transfer in fast page mode requires 3 clocks for the initial transfer and 2 clocks for all secondary writes. You can program the DCTR to generate slower fast page mode transfers.

Figure 10-9 shows the timing of a page being opened by a word write transfer to a 16-bit port in Fast Page Mode. The first word write transfer is followed by a page-hit word write transfer. The timing of the page-hit write transfer is the same regardless of whether the page was opened by a burst read, burst write, nonburst read, or nonburst write transfer.

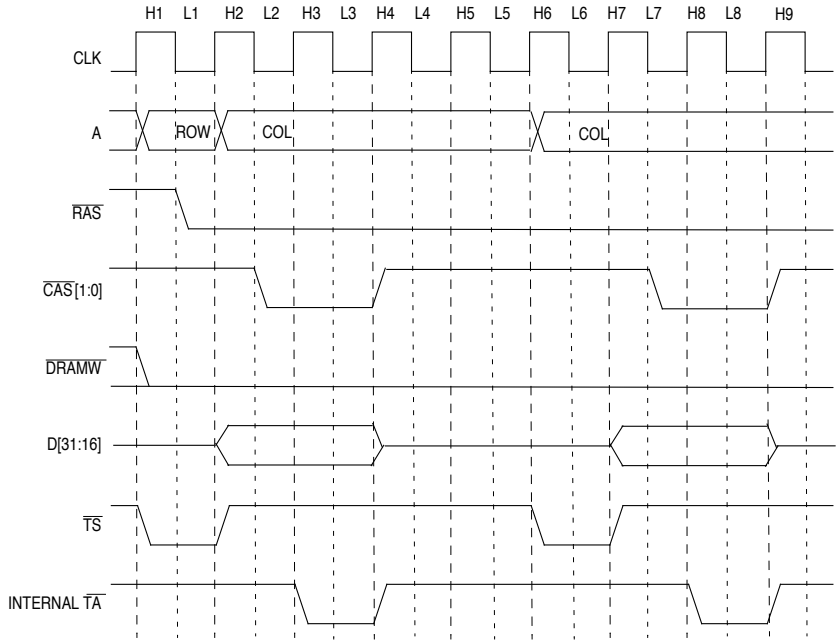

Figure 10-9. Word Write Transfer Followed by a Page-Hit Word Write Transfer in Fast Page Mode with 16-bit DRAM

Clock H1

The first word write transfer starts in H1. During H1, the MCF5206 drives the row address on A[27:9], drives $\overline{\text{DRAMW}}$ low indicating a DRAM write transfer, drives SIZ[1:0] to $2 indicating a word transfer, and asserts $\overline{\text{TS}}$.

Clock L1

The MCF5206 asserts $\overline{\text{RAS}}$ to indicate the row address is valid on A[27:9].

Clock H2

The MCF5206 negates $\overline{\text{TS}}$, drives the column address on A[27:9], and begins driving the data on D[31:16].

Clock L2

The MCF5206 asserts $\overline{\text{CAS}}$[1:0] to indicate the column address is valid on A[27:9].

Clock H3

The internal transfer acknowledge asserts to indicate that the word write transfer will be completed on the next rising edge of CLK.

Clock H4

The MCF5206 negates the internal transfer acknowledge, and $\overline{\text{CAS}}$[1:0], ending the first word write transfer. At this point, the new page has been opened; therefore, the MCF5206 continues to assert $\overline{\text{RAS}}$. The negation of $\overline{\text{CAS}}$[1:0] begins the $\overline{\text{CAS}}$ precharge. When the write is completed, the MCF5206 three-states D[31:0].

Clock H6

Clock H6 is the earliest the next transfer initiated by the ColdFire core can start. In this case, a page-hit word write transfer is shown. The word write transfer starts in H6. During H6, the MCF5206 drives the column address on A[27:9], drives $\overline{\text{DRAMW}}$ low indicating a DRAM write transfer, drives SIZ[1:0] to $2 indicating a word transfer, and asserts $\overline{\text{TS}}$.

Clock H7

Clock H7 is the same as Clock H2.

Clock L7

Clock L7 is the same as Clock L2.

Clock H8

Clock H8 is the same as Clock H3.

Clock H9

The MCF5206 negates the internal transfer acknowledge, and $\overline{\text{CAS}}$[1:0], ending the second word write transfer. Because the DRAM bank is in fast page mode, the MCF5206 continues to assert $\overline{\text{RAS}}$. The negation of $\overline{\text{CAS}}$[1:0] begins the $\overline{\text{CAS}}$ precharge. When the write is completed, the MCF5206 three-states D[31:0].

10.3.4.4 PAGE MISS TRANSFER IN FAST PAGE MODE.

There is a potential performance penalty when using fast page mode. If a DRAM transfer misses the open page, the start of the transfer will be delayed while $\overline{\text{RAS}}$ precharges. Therefore, fast page mode can increase performance when many successive transfers hit in the same page, but can also decrease performance when successive transfers hit in different pages.

In cases where a page is open in one bank and a transfer hits in the other bank, the transfer will not be delayed because the second bank has already been precharged.

The fastest possible page miss transfer in Fast page mode requires 4 clocks. The total number of clocks in a page miss transfer is the $\overline{RAS}$ precharge time, which causes the start of the transfer to be delayed (1 cycle for the fastest page miss transfer), plus the length of a fast page mode transfer to a new page (3 cycles for the fastest page miss transfer).

Figure 10-8 shows the timing of a page miss transfer in fast page mode. In this example, a page is opened by a byte read transfer to an 8-bit port. Then a second byte read transfer starts internally which misses the open page. Therefore, $\overline{RAS}$ must be precharged and a new page must be opened. The timing of the page-miss write transfer is the same as the timing of a page-miss read transfer.

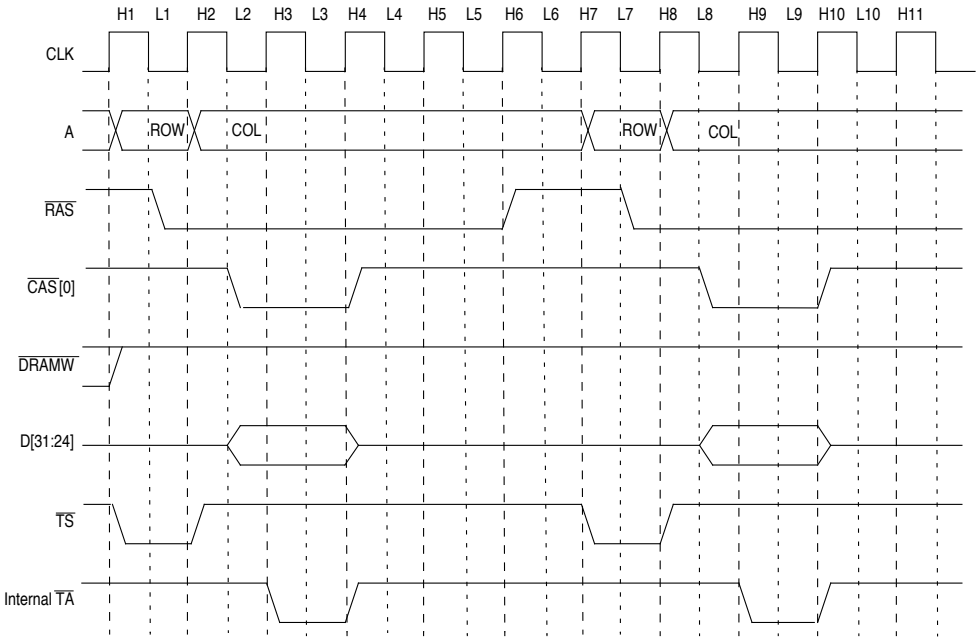

Figure 10-10. Byte Read Transfer Followed by a Page-Miss Byte Read Transfer in Fast Page Mode with 8-Bit DRAM

Clock H1

The first DRAM read transfer starts in H1. During H1, the MCF5206 drives the row address on A[27:9], drives $\overline{\text{DRAMW}}$ high indicating a DRAM read transfer, drives SIZ[1:0] to $1 indicating a byte transfer, and asserts $\overline{\text{TS}}$.

Clock L1

The MCF5206 asserts $\overline{\text{RAS}}$ to indicate the row address is valid on A[27:9].

Clock H2

The MCF5206 negates $\overline{\text{TS}}$, and drives the column address on A[27:9].

Clock L2

The MCF5206 asserts $\overline{\text{CAS}}$[0] to indicate the column address is valid on A[27:9]. At this point the DRAM will turn on its output drivers and begin driving data on D[31:24].

Clock H3

The internal transfer acknowledge asserts to indicate that the byte read transfer will be completed and data on D[31:24] will be registered on the next rising edge of CLK.

Clock H4

The MCF5206 negates the internal transfer acknowledge, and $\overline{\text{CAS}}$[0], ending the first byte read transfer. At this point, the new page has been opened; therefore, the MCF5206 continues to assert $\overline{\text{RAS}}$. Once $\overline{\text{CAS}}$[0] is negated, the DRAM disables its output drivers and D[31:0] is three-stated. The negation of $\overline{\text{CAS}}$[0] begins the $\overline{\text{CAS}}$ precharge.

Clock H5/L5

A byte read transfer to the same DRAM bank is generated internally by the ColdFire core. This transfer misses the open page.

Clock H6

The ColdFire core initiated a DRAM transfer on the previous cycle that misses the open page. Therefore, the MCF5206 negates $\overline{\text{RAS}}$, beginning the $\overline{\text{RAS}}$ precharge. Once the $\overline{\text{RAS}}$ precharge time has been reached, a transfer to a new page can start.

Clock H7

The byte read transfer to a new page starts in H7. During H7, the MCF5206 drives the row address on A[27:9], drives $\overline{\text{DRAMW}}$ high indicating a DRAM read transfer, drives SIZ[1:0] to $1 indicating a byte transfer, and asserts $\overline{\text{TS}}$.

Clock L7

The $\overline{RAS}$ precharge time has been met, so the MCF5206 asserts $\overline{RAS}$ is to indicate the row address is valid on A[27:9].

Clock H8

Clock H8 is the same as Clock H2.

Clock L8

Clock L8 is the same as Clock L2.

Clock H9

Clock H9 is the same as Clock H3.

Clock H10

Clock H10 is the same as Clock H4.

10.3.4.5 BUS ARBITRATION. If the MCF5206 loses bus mastership while a page is open ($\overline{RAS}$ is asserted), $\overline{RAS}$ will be precharged. The $\overline{RAS}$ precharge timing depends on whether an active fast page mode DRAM transfer is in progress, whether a nonDRAM transfer is in progress, or whether the external bus is idle.

If the BL bit in the SIMR is cleared and $\overline{BG}$ is negated while an active fast page mode DRAM transfer is in progress, $\overline{BD}$ will remain asserted until the transfer is complete. Once the DRAM transfer completes, the MCF5206 will negate $\overline{BD}$ and begin precharging $\overline{RAS}$.

In the case where the BL bit in the SIMR is cleared and $\overline{BG}$ is negated while a nonDRAM transfer is in progress and a page is open, the MCF5206 will begin precharging $\overline{RAS}$ on the cycle following the negation of $\overline{BG}$, even though $\overline{BD}$ remains asserted until the completion of the nonDRAM transfer.

If the BL bit in the SIMR is cleared and $\overline{BG}$ is negated while the external bus is idle and a page is open, the MCF5206 will negate $\overline{BD}$ and begin precharging $\overline{RAS}$ on the cycle following the negation of $\overline{BG}$.

When the BL bit in the SIMR is set to 1 and $\overline{BG}$ is asserted, the bus is locked with the MCF5206. If $\overline{BG}$ is negated while the bus is locked and a page is open, $\overline{RAS}$ and $\overline{BD}$ will remain asserted, because the MCF5206 maintains bus mastership regardless of $\overline{BG}$ when the bus is locked.

NOTE

fast page mode is not supported for alternate master DRAM transfers. A DRAM bank programmed for fast page mode, will

operate in fast page mode for ColdFire core initiated transfers, but will operate in burst page mode for alternate master initiated transfers.

Figure 10-11 shows the effect of bus arbitration on the DRAM signals when the external bus is idle and a page is open in fast page mode.

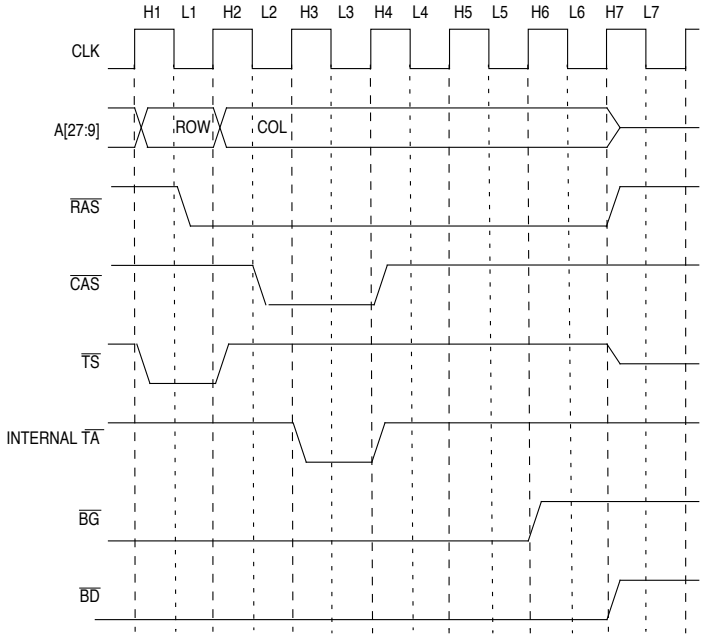

Figure 10-11. Bus Arbitration in Fast Page Mode

Clock H1

A Fast Page Mode transfer starts in H1. During H1, the MCF5206 drives the row address on A[27:9], and asserts $\overline{TS}$.

Clock L1

The MCF5206 asserts $\overline{RAS}$ to indicate the row address is valid on A[27:9].

Clock H2

The MCF5206 negates $\overline{TS}$, and drives the column address on A[27:9].

Clock L2

The MCF5206 asserts $\overline{CAS}$ to indicate the column address is valid on A[27:9].

Clock H3

The internal transfer acknowledge asserts to indicate that the current transfer will be completed on the next rising edge of CLK.

Clock H4

The MCF5206 negates the internal transfer acknowledge, and $\overline{CAS}$, ending the transfer. At this point, a page has been opened; therefore, the MCF5206 continues to assert $\overline{RAS}$. The negation of $\overline{CAS}$ begins the $\overline{CAS}$ precharge.

Clock H6

After the bus has idled for two clocks, $\overline{BG}$ is negated (while the BL bit in the SIMR is cleared).

Clock H7

The MCF5206 then three-states the external bus signals, negates $\overline{RAS}$ (closing the page), and negates $\overline{BD}$, relinquishing mastership of the bus. The negation of $\overline{RAS}$ begins the $\overline{RAS}$ precharge.

10.3.5 Burst Page-Mode Operation

Burst page mode performs fast page mode transfers only for burst transfers. A burst transfer to DRAM will occur any time the operand size is larger than the DRAM bank port size (e.g., line transfer to a 32-bit port, longword transfer to an 8-bit port). After completing the burst, the MCF5206 negates $\overline{RAS}$, closing the page. Because all secondary transfers of a burst are guaranteed to be page hits, a page miss will never occur in burst page mode. Nonburst transfers will occur as in normal mode. Therefore, burst page mode will always give the same or better performance than normal mode.

The timing of read and write transfers is identical in burst page mode, with the exception of when the DRAM drives data on reads and when the MCF5206 drives data on writes.

The fastest possible burst transfer in burst page mode requires three clocks for the first transfer and two clocks on the secondary transfers. The fastest possible nonburst transfer in burst page mode requires three clocks. You can program the DCTR to generate slower burst page mode transfers.

Figure 10-12 shows a longword write transfer followed by a word read transfer to a 16-bit port with burst page mode enabled for the bank. The burst longword write transfer is handled as in fast page mode with the initial word transfer of the burst taking three cycles and the secondary word transfer taking two cycles. However, in burst page mode, the MCF5206 precharges $\overline{RAS}$ once the burst transfer is complete. The second transfer (a word read) is executed as in normal mode as it is not a burst transfer.

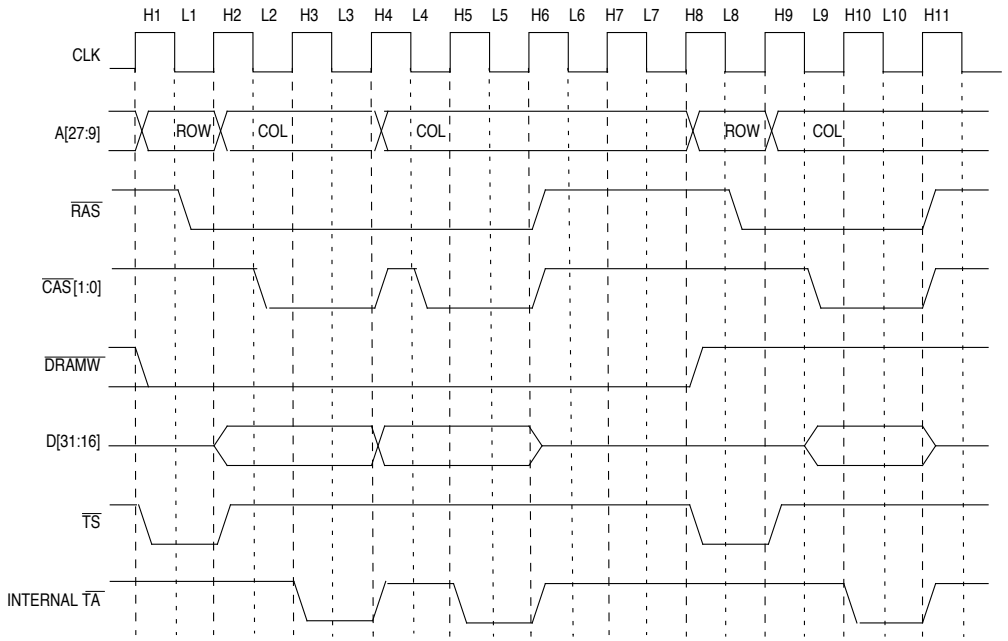

Figure 10-12. Longword Write Transfer Followed by a Word Read Transfer in Burst Page Mode with 16-Bit DRAM

Clock H1

The first word write transfer of the longword burst starts in H1. During H1, the MCF5206 drives the row address on A[27:9], drives $\overline{\text{DRAMW}}$ low indicating a DRAM write transfer, drives SIZ[1:0] to $0 indicating a longword transfer, and asserts $\overline{\text{TS}}$.

Clock L1

The MCF5206 asserts $\overline{\text{RAS}}$ to indicate the row address is valid on A[27:9].

Clock H2

The MCF5206 negates $\overline{\text{TS}}$, drives the column address on A[27:9], and begins driving the data on D[31:16].

Clock L2

The MCF5206 asserts $\overline{\text{CAS}}$[1:0] to indicate the column address is valid on A[27:9].

Clock H3

The internal transfer acknowledge asserts to indicate that the first word transfer of the longword burst will be completed on the next rising edge of CLK.

Clock H4

The MCF5206 negates the internal transfer acknowledge, and $\overline{CAS}$[1:0], ending the first word write transfer of the longword burst. At this point, the new page has been opened; therefore, the MCF5206 continues to assert $\overline{RAS}$. The negation of $\overline{CAS}$[1:0] begins the $\overline{CAS}$ precharge. The MCF5206 drives the next column address on A[27:9] and the next data on D[31:16].

Clock L4

Clock L4 is the same as Clock L2.

Clock H5

Clock H5 is the same as Clock H3.

Clock H6

The MCF5206 negates the internal transfer acknowledge, $\overline{RAS}$, and $\overline{CAS}$[1:0], ending the final write transfer of the longword burst. Because the bank is in burst page mode, MCF5206 precharges $\overline{RAS}$ at the end of the burst. The negation of $\overline{RAS}$ begins the $\overline{RAS}$ precharge. When the burst write is completed, the MCF5206 three-states D[31:0].

Clock H8

Clock H8 is the earliest the next transfer initiated by the ColdFire core can start. Because this next DRAM cycle is a nonburst word read transfer, it will be handled as a normal mode transfer. During Clock H8, the MCF5206 drives the row address on A[27:9], drives $\overline{DRAMW}$ high indicating a DRAM read transfer, drives SIZ[1:0] to $2 indicating a word transfer, and asserts $\overline{TS}$.

Clock L8

The MCF5206 asserts $\overline{RAS}$ to indicate the row address is valid on A[27:9].

Clock H9

The MCF5206 negates $\overline{TS}$, and drives the column address on A[27:9]

Clock L9

The MCF5206 asserts $\overline{CAS}$[1:0] to indicate the column address is valid on A[27:9]. At this point the DRAM will turn on its output drivers and begin driving the data on D[31:16].

Clock H10

The internal transfer acknowledge asserts to indicate that the current transfer will be completed and the data on D[31:16] will be registered on the next rising edge of CLK.

Clock H11

The MCF5206 registers the read data driven by the DRAM, and negates the internal transfer acknowledge, $\overline{RAS}$ and $\overline{CAS}$[1:0], ending the word read transfer. This begins the $\overline{RAS}$ precharge. Once $\overline{CAS}$ is negated, the DRAM disables its output drivers and D[31:0] is three-stated.

10.3.6 Extended Data-Out (EDO) DRAM Operation

Extended data-out (EDO) DRAMs do not three-state their output drivers at the negation of $\overline{CAS}$ on page read transfers as do fast-page-mode DRAMs. Instead, data remains valid until some time (typically 5 ns) after the next falling edge of $\overline{CAS}$. This allows $\overline{CAS}$ to be precharged without the output data going invalid. The result is that a system using slower, less expensive EDO DRAM can achieve the same performance as a system using faster, more expensive fast-page-mode DRAMs.

The MCF5206 supports EDO DRAM with a $\overline{CAS}$ timing that takes advantage of the read data remaining valid after $\overline{CAS}$ negates. To enable the EDO $\overline{CAS}$ timing for both DRAM banks, set the EDO Enable bit in the DCTR to 1. When set to 1, $\overline{CAS}$ negates one-half clock cycle earlier for fast-page-mode and burst-page-mode transfers than when the EDO Enable bit is cleared. At higher clock frequencies, the EDO $\overline{CAS}$ timing allows slower, less expensive EDO DRAMs to be used, since the $\overline{CAS}$ precharge starts before data is registered on read transfers. For the fastest timing in fast page mode or burst page mode, having the EDO Enable bit set gives one clock of $\overline{CAS}$ precharge time, rather than one-half of a clock with the EDO Enable bit cleared.

Since EDO DRAM continues to drive data after a read as long as $\overline{RAS}$ is asserted, be careful with the system design using EDO DRAM to ensure bus contention does not occur when a nonDRAM transfer occurs while a page is open in fast page mode.

NOTE

Failure to use normal mode or burst page mode with EDO DRAM without external circuitry to control the DRAM output drivers could result in damage to the MCF5206 and the system.

Figure 10-13 shows the timing of a word read in Fast Page Mode followed by a page miss word read using 8-bit wide EDO DRAM (the EDO bit in the DCTR is set).

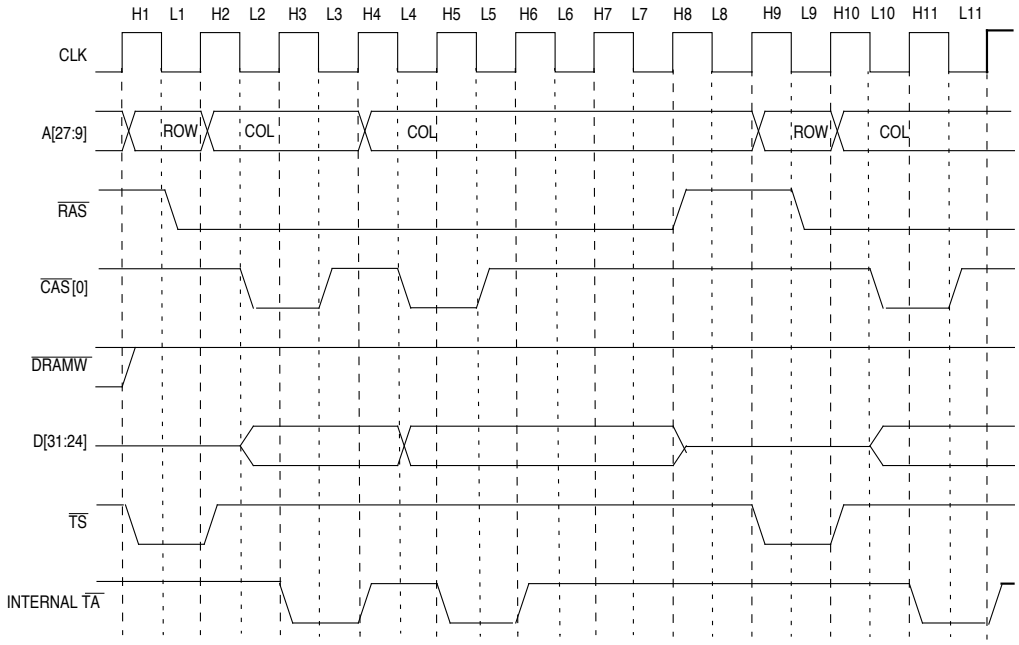

Figure 10-13. Word Read Transfer Followed by a Page Miss Byte Read Transfer in Fast Page Mode with 8-Bit EDO DRAM

Clock H1

The first byte read transfer of the burst word transfer starts in H1. During H1, the MCF5206 drives the row address on A[27:9], drives $\overline{\text{DRAMW}}$ high indicating a DRAM write transfer, drives SIZ[1:0] to $2 indicating a byte transfer, and asserts $\overline{\text{TS}}$.

Clock L1

The MCF5206 asserts $\overline{\text{RAS}}$ to indicate the row address is valid on A[27:9].

Clock H2

The MCF5206 negates $\overline{\text{TS}}$, drives the column address on A[27:9].

Clock L2

The MCF5206 asserts $\overline{\text{CAS}}$[0] to indicate the column address is valid on A[27:9]. At this point the EDO DRAM will turn on it's output drivers and begin driving data on D[31:24].

Clock H3

The internal transfer acknowledge asserts to indicate that the first byte read transfer of the word burst will be completed and the data on D[31:24] will be registered on the next rising edge of CLK.

Clock L3

With EDO DRAM, data is driven continuously on a read after the falling edge of $\overline{CAS}$ until the next falling edge of $\overline{CAS}$ or until the rising edge of $\overline{RAS}$. This allows the MCF5206 to negate $\overline{CAS}$[0] on L3 to allow more $\overline{CAS}$ precharge time. The negation of $\overline{CAS}$[0] begins the $\overline{CAS}$ precharge.

Clock H4

The MCF5206 negates the internal transfer acknowledge, ending the first byte read transfer of the word burst. At this point, the new page has been opened; therefore, the MCF5206 continues to assert $\overline{RAS}$. The MCF5206 drives the next column address on A[27:9].

Clock L4

The MCF5206 asserts $\overline{CAS}$[0] to indicate the column address is valid on A[27:9]. At this point, the EDO DRAM begins driving the data on D[31:24].

Clock H5

Clock H5 is the same as Clock H3.

Clock L5

Clock L5 is the same as Clock L3.

Clock H6

The MCF5206 negates the internal transfer acknowledge, ending the final byte read transfer of the word burst. Because the bank is in fast page mode, MCF5206 continues to assert $\overline{RAS}$. Because $\overline{RAS}$ remains asserted, the EDO DRAM continues to drive the data from the previous read transfer on D[31:24].

Clock H7/L7

A byte read transfer to the same DRAM bank is generated internally by the ColdFire core. This transfer misses the open page.

Clock H8

The ColdFire core initiated a DRAM transfer on the previous cycle that missed the open page. Therefore, the MCF5206 negates $\overline{RAS}$, beginning the $\overline{RAS}$ precharge. Once the

$\overline{RAS}$ precharge time has been reached, a transfer to a new page can start. Once $\overline{RAS}$ is negated, the EDO DRAM disables its output drivers and D[31:0] is three-stated.

Clock H9

The byte read transfer to a new page starts in H9. During H9, the MCF5206 drives the row address on A[27:9], drives $\overline{DRAMW}$ high indicating a DRAM read transfer, drives SIZ[1:0] to $1 indicating a byte transfer, and asserts $\overline{TS}$.

Clock L9

Now that the $\overline{RAS}$ precharge time has been reached, the MCF5206 asserts $\overline{RAS}$ is to indicate the row address is valid on A[27:9].

Clock H10

Clock H10 is the same as Clock H2.

Clock L10

Clock L10 is the same as Clock L2.

Clock H11

Clock H11 is the same as Clock H3.

Clock H12

The MCF5206 negates the internal transfer acknowledge, ending the byte-read transfer. Because the bank is in fast page mode, MCF5206 continues to assert $\overline{RAS}$. Because $\overline{RAS}$ remains asserted, the EDO DRAM continues to drive the data from the previous read transfer on D[31:24].

10.3.7 Refresh Operation

The DRAMC supports $\overline{CAS}$-before-$\overline{RAS}$ refresh. Refresh cycles can be generated while nonDRAM transfers are actively using the external bus. Only transfers accessing the DRAM banks will delay a refresh cycle. Both DRAM banks are refreshed on each refresh cycle.

The value stored in the RC field of the DCRR determines the rate at which the refresh controller internally requests refreshes in the DRAMC. The DRAMC will not immediately initiate a refresh cycle if a DRAM transfer is occurring when the internal refresh request is made. The DRAMC will wait until the active DRAM transfer is complete and will then initiate the DRAM refresh cycle. Refresh cycles will occur immediately after the internal refresh request is made during idle bus cycles and during nonDRAM transfers.

NOTE

Add margin when determining the value to program into the RC field of the DCRR so that a refresh cycle delayed by the longest possible DRAM transfer will not violate the refresh rate specified for the DRAMs being used.

Programming the RC field in the DCRR to $000 will cause internal refresh requests to occur at the slowest rate—once every 65,536 system clock cycles. Programming the RC field in the DCRR to $001 will cause internal refresh requests to occur at the fastest rate—once every 16 system clocks. If multiple refresh requests occur while waiting for a DRAM transfer to finish, only one refresh cycle will be generated.

Writing to the DCRR will cause an internal refresh request to occur and the refresh counter to be reloaded. If the DCRR is written while a refresh request is pending, only one refresh cycle will be generated. If the DCRR is written while a refresh cycle is in progress, another refresh cycle will not be generated after the one in progress completes.

The refresh period is the amount of time between internal refresh requests. The refresh period can be calculated from the value programmed in the RC field of the DCRR using the following equations:

For RC>$000:

Refresh period = RC x16 x (1/system clock frequency)

For RC=$000:

Refresh period = 65536 x (1/system clock frequency)

When the DRAMC initiates a refresh cycle, it will delay any DRAM transfer initiated by the ColdFire core or by an alternate master until the $\overline{RAS}$ precharge is complete at the end of refresh cycle. If a DRAM transfer is initiated by the ColdFire core while a refresh cycle is in progress and the MCF5206 is not the bus master, bus request ($\overline{BR}$) will not be asserted until after the refresh completes.

A master reset will terminate any active refresh cycle and will reset the refresh controller. Master reset is required on all power-on resets. During a master reset, refresh cycles will not occur; after a master reset, refreshes will occur at the slowest rate (DCRR is initialized to $0000).

NOTE

During a master reset, the DCCR is reset to $000 (giving the slowest refresh rate) and the DCTR is reset to $0000 (giving the fastest waveform timing). After a master reset, the initialization sequence should program the DRAMC Refresh Register (DCRR) and the DRAMC Timing Register (DCTR)

such that refresh cycles are generated at the required rate and with the required timing for the DRAM in the system. In general, DRAMs require an initial pause after power-up and require a minimum number of DRAM cycles to be run before the DRAM is ready for use. This initialization sequence must be handled through software.

Normal reset will not affect a refresh cycle in progress and will not reset the refresh controller. Refreshes will occur during a normal reset with the timing specified in the DCTR and at the rate specified in the DCRR.

10.3.8 Alternate Master Use of the DRAM Controller

The DRAMC can support alternate master-initiated transfers. When an alternate master is the bus master, the MCF5206 registers all available address signals, R/$\overline{W}$, and SIZ[1:0] on the rising edge of clock when $\overline{TS}$ is asserted. Based on the address, direction, and data size, the DRAMC will assert $\overline{RAS}$, $\overline{CAS}$, $\overline{DRAMW}$, and conditionally drive the address bus.

NOTE

If you do not want the MCF5206 DRAMC to respond on alternate master transfers, $\overline{TS}$ should not be asserted to the MCF5206 during alternate master transfers. The MCF5206 will, however, continue to generate DRAM refresh cycles while the bus is granted to an alternate master.

NOTE

The driving of the data on writes and the latching of data on reads based on the data size and port size of the DRAM is the responsibility of the alternate master. The MCF5206 will not drive the data bus when it is not master of the external bus.

The MCF5206 can delay the access to DRAM for an alternate master initiated transfer if a refresh request is pending or if the programmed $\overline{RAS}$ precharge time has not been reached. If there is a refresh cycle in progress or if there is a refresh request pending when an alternate master starts a DRAM transfer, the MCF5206 will not start driving the row address and assert $\overline{RAS}$ until the $\overline{RAS}$ precharge time has been reached after completing the refresh cycle. If a refresh request occurs during an alternate master DRAM transfer, the refresh cycle will be delayed until the alternate master DRAM transfer is completed. If the programmed $\overline{RAS}$ precharge time from the previous DRAM transfer has not been reached, the MCF5206 will not start driving the row address and assert $\overline{RAS}$ until the precharge time has been reached.

For alternate master DRAM transfers, the MCF5206 will drive $\overline{TA}$ as an output. $\overline{TA}$ is asserted to signify the end of each transfer (or subtransfer in the case of a burst). The assertion of $\overline{TA}$ can be used for latching data on read transfers and can also be used by

the alternate master to trigger the driving of new write data for successive transfers during bursts.

When using the MCF5206 to multiplex the address for alternate master DRAM transfers (DAEM bit in the DCTR is set), the alternate master must stop driving the address bus during the clock cycle after $\overline{TS}$ is asserted. This allows the MCF5206 to drive the row address and the column address on A[27:9] at the appropriate times. If the alternate master cannot three-state the address bus, the driving of the address by the MCF5206 should be disabled and the address multiplexing for alternate master transfers must be handled in the external system.

If address multiplexing for alternate master transfers is to be handled in the external system, the DRAMC must be configured to three-state the address bus during these transfers by clearing the DAEM bit in the DCTR. This will not affect the operation of $\overline{TA}$, $\overline{RAS}$, $\overline{CAS}$, or $\overline{DRAMW}$ during alternate master DRAM transfers.

NOTE

The MCF5206 does not drive the address for alternate master chip-select or default memory transfers.

10.3.8.1 ALTERNATE MASTER NONBURST TRANSFER IN NORMAL MODE. An alternate master nonburst transfer to DRAM will be generated when the operand size is the same or smaller than the DRAM port size (e.g., longword transfer to a 32-bit port or byte transfer to a 16-bit port). The alternate master must assert $\overline{TS}$ at the start of all nonburst transfers.

The timing of nonburst reads and nonburst writes is identical in normal page mode, with the exception of when the DRAM drives data on reads and when the alternate master drives data on writes.

The fastest possible nonburst transfer in normal mode requires 5 clocks. You can program the DCTR to generate slower normal mode transfers.

Figure 10-14 illustrates the timing of an alternate master DRAM byte read transfer followed by a byte write transfer to a 8-bit port in normal mode.

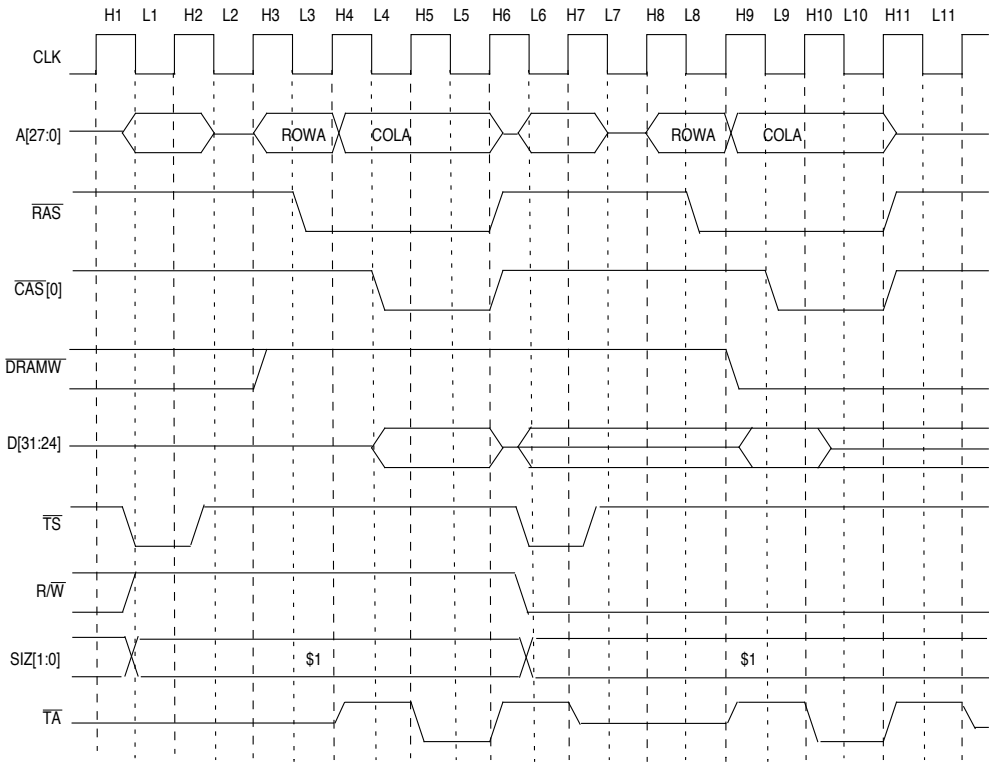

Figure 10-14. Alternate Master Byte Read Transfer Followed by Byte Write Transfer in Normal Mode with 16-Bit DRAM

Clock H1/L1

An alternate master is the current bus master. The alternate master starts a DRAM transfer by driving A[27:0], driving R/$\overline{W}$ high indicating a read transfer, driving $\overline{SIZ}$[1:0] to $1 indicating a byte transfer, and asserting $\overline{TS}$. These inputs to the MCF5206 must be set up with respect to the rising edge of CLK H2.

Clock H2

On the rising edge of CLK when $\overline{TS}$ is asserted, the MCF5206 registers the address and attribute signals. The MCF5206 will internally decode these signals and determine if the alternate master transfer is a DRAM access. The alternate master negates $\overline{TS}$ and must three-state A[27:0] after the rising edge of CLK H2, if the internal address multiplexing is to be used.

Clock H3

The MCF5206 has determined that the alternate master transfer is a DRAM access, so the MCF5206 drives A[27:0] with the same value as was registered on the rising edge of H2. A[27:9] will be the DRAM row address. The MCF5206 also drives $\overline{\text{DRAMW}}$ high, indicating a DRAM read cycle.

Clock L3

The MCF5206 asserts $\overline{\text{RAS}}$ to indicate the row address is valid on A[27:9].

Clock H4

The MCF5206 internally multiplexes the address and drives out the column address on A[27:9]. The MCF5206 also actively drives $\overline{\text{TA}}$ negated.

Clock L4

The MCF5206 asserts $\overline{\text{CAS}}$[0] to indicate the column address is valid on A[27:9]. At this point the DRAM will turn on its output drivers and begin driving the data on D[31:24].

Clock H5

The MCF5206 asserts the $\overline{\text{TA}}$ signal to indicate that the byte read transfer will be completed and the read data will be valid on D[31:24] on the next rising edge of CLK.

Clock H6

The MCF5206 then negates $\overline{\text{RAS}}$, $\overline{\text{CAS}}$[0], and $\overline{\text{TA}}$ and three-states A[27:0], ending the byte-read transfer. The negation of $\overline{\text{RAS}}$ starts the $\overline{\text{RAS}}$ precharge. Once A[27:0] has three-stated, the alternate master can start another transfer. In this case, the alternate master starts a DRAM byte write transfer immediately by driving A[27:0], driving R/$\overline{\text{W}}$ low indicating a write transfer, driving $\overline{\text{SIZ}}$[1:0] to $1 indicating a byte transfer, and asserting $\overline{\text{TS}}$. The alternate master must drive the data in the correct byte lanes based on the data size and the port size of the DRAM, and must drive the data to meet the timing specifications of the DRAM. In this case, the alternate master should drive the write data on D[31:24].

Clock H7

The MCF5206 three-states $\overline{\text{TA}}$. On the rising edge of CLK where $\overline{\text{TS}}$ is asserted, the MCF5206 registers the address and attribute signals. The MCF5206 will internally decode these signals and determine if the alternate master transfer is a DRAM access. The alternate master must three-state A[27:0] after the rising edge of CLK H2, if the internal address multiplexing is to be used.

Clock H8

The MCF5206 has determined that the alternate master transfer is a DRAM access, so the MCF5206 drives the A[27:0] with the same value as was registered on the rising edge of H2. A[27:9] will be the row address for the DRAM. The MCF5206 also drives $\overline{\text{DRAMW}}$ low, indicating a DRAM write cycle.

Clock L8

Clock L8 is the same as Clock L3.

Clock H9

Clock H9 is the same as Clock H4.

Clock L9

The MCF5206 asserts $\overline{\text{CAS}}$[0] to indicate the column address is valid on A[27:9]. The alternate master must set up and hold the data with respect to the falling edge of $\overline{\text{CAS}}$[0] based on the DRAM specifications.

Clock H10

The MCF5206 asserts the $\overline{\text{TA}}$ signal to indicate that the byte write transfer will be completed on the next rising edge of CLK.

Clock H11

The MCF5206 then negates $\overline{\text{RAS}}$, $\overline{\text{CAS}}$[0], and $\overline{\text{TA}}$, and three-state the address bus, ending the byte write transfer. The negation of $\overline{\text{RAS}}$ starts the $\overline{\text{RAS}}$ precharge. Once A[27:0] has three-stated, the alternate master can start another transfer.

Clock H12

The MCF5206 three-states $\overline{\text{TA}}$.

10.3.8.2 ALTERNATE MASTER BURST TRANSFER IN NORMAL MODE. A burst transfer to DRAM will be generated when the operand size is larger than the DRAM bank port size (e.g., line transfer to a 32-bit port, longword transfer to an 8-bit port). On DRAM burst transfers, the alternate master should assert $\overline{\text{TS}}$ only once. The start of the secondary transfers of a burst is delayed by the DRAMC until the programmed $\overline{\text{RAS}}$ precharge time is met.

The timing of alternate master burst reads and burst writes is identical in normal page mode, with the exception of when the DRAM drives data on reads and when the alternate master drives data on writes.

The fastest possible alternate master burst transfer in normal mode requires 5 clocks for the first transfer of the burst and 4 clocks for the secondary transfers (including a 1.5 clock $\overline{RAS}$ precharge time). You can program the DCTR to generate slower normal mode transfers.

Figure 10-15 illustrates the timing of a alternate master longword write transfer to a 16-bit DRAM in normal mode. The timing of the first transfer of the burst operates the same as the nonburst case. After the first transfer of the burst completes, $\overline{TA}$ is negated and the row address is driven again by the MCF5206. The MCF5206 asserts $\overline{RAS}$ after the $\overline{RAS}$ precharge time is met and the transfer completes the same as in the nonburst case. Driving the write data in the correct byte lanes at the proper time to meet the specifications of the DRAM is the responsibility of the alternate master.

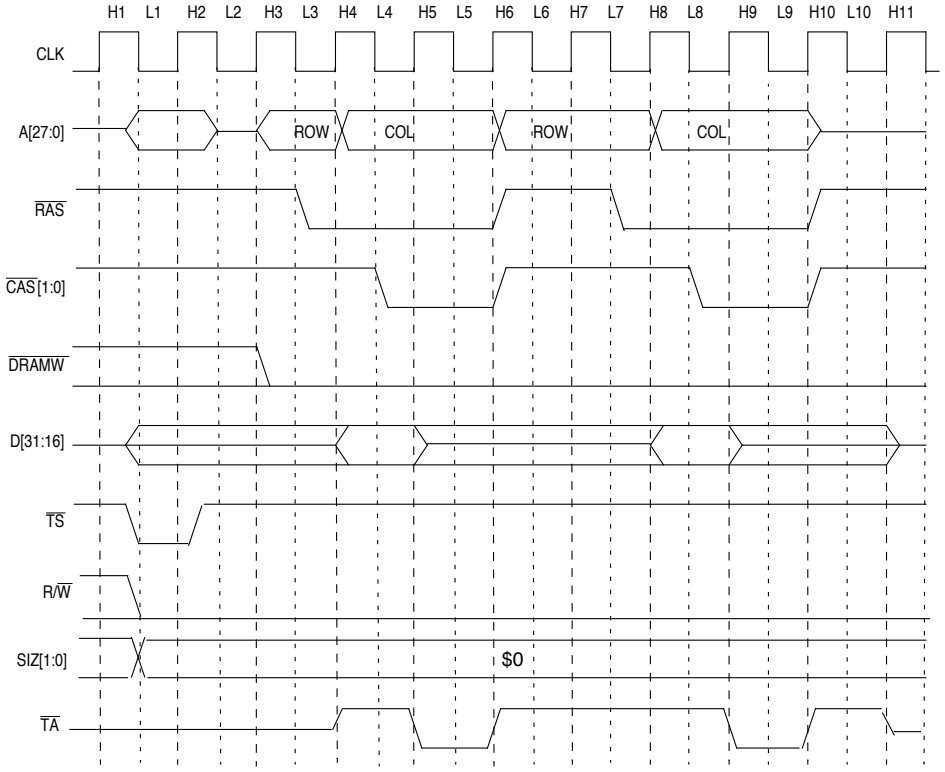

Figure 10-15. Alternate Master Longword Write Transfer in Normal Mode with 16-Bit DRAM

Clock H1/L1

An alternate master is the current bus master. The alternate master starts a DRAM transfer by driving A[27:0], driving R/$\overline{W}$ low indicating a write transfer, driving $\overline{SIZ}$[1:0] to $0 indicating a longword transfer, and asserting $\overline{TS}$. These inputs to the MCF5206 must be set up with respect to the rising edge of CLK H2. The alternate master must drive the

data in the correct byte lanes based on the data size and the port size of the DRAM, and must drive the data to meet the timing specifications of the DRAM. In this case, the alternate master should drive the write data on D[31:16].

Clock H2

On the rising edge of CLK when $\overline{TS}$ is asserted, the MCF5206 registers the address and attribute signals. It will internally decode these signals and determine if the alternate master transfer is a DRAM access. The alternate master negates $\overline{TS}$ and must three-state A[27:0] after the rising edge of CLK H2, if the internal address multiplexing is to be used.

Clock H3

The MCF5206 has determined that the alternate master transfer is a DRAM access, so the MCF5206 drives A[27:0] with the same value as was registered on the rising edge of H2. A[27:9] will be the DRAM row address. The MCF5206 also drives $\overline{DRAMW}$ low indicating a DRAM write cycle.

Clock L3

The MCF5206 asserts $\overline{RAS}$ to indicate the row address is valid on A[27:9].

Clock H4

The MCF5206 internally multiplexes the address and drives out the column address on A[27:9]. The MCF5206 also actively drives $\overline{TA}$ negated.

Clock L4

The MCF5206 asserts $\overline{CAS}$[1:0] to indicate the column address is valid on A[27:9]. The alternate master must set up and hold the first word of data on D[31:16] with respect to the falling edge of $\overline{CAS}$[1:0] based on the DRAM specifications.

Clock H5

The MCF5206 asserts the $\overline{TA}$ signal to indicate that the first word write transfer of the longword burst will be completed on the next rising edge of CLK.

Clock H6

The MCF5206 negates $\overline{RAS}$, $\overline{CAS}$[1:0], and $\overline{TA}$, ending the first word transfer of the longword burst. The negation of $\overline{RAS}$ starts the $\overline{RAS}$ precharge. The MCF5206 drives the row address again for second word transfer of the longword burst write.

Clock L7

Once the $\overline{RAS}$ precharge time has been met, the MCF5206 asserts $\overline{RAS}$ to indicate the row address is valid on A[27:9].

Clock H8

The MCF5206 internally increments and multiplexes the address and drives out the column address on A[27:9] for the second word transfer of the longword burst write.

Clock L8

Clock L8 is the same as Clock L4. The MCF5206 asserts $\overline{CAS}$[1:0] to indicate the column address is valid on A[27:9]. The alternate master must set up and hold the second word of data on D[31:16] with respect to the falling edge of $\overline{CAS}$[1:0] based on the DRAM specifications.

Clock H9

Clock H9 is the same as Clock H5. The MCF5206 asserts the $\overline{TA}$ signal to indicate that the second word write transfer of the longword burst will be completed on the next rising edge of CLK.

Clock H10

The MCF5206 negates $\overline{RAS}$, $\overline{CAS}$[1:0], and $\overline{TA}$, and three-states A[27:0], ending the second word transfer of the longword burst. The negation of $\overline{RAS}$ starts the $\overline{RAS}$ precharge. Once A[27:0] has three-stated, the alternate master can start another transfer.

Clock H11

The MCF5206 three-states $\overline{TA}$.

10.3.8.3 ALTERNATE MASTER BURST TRANSFER IN BURST PAGE MODE. Burst page mode does fast page mode transfers only for burst transfers. A burst transfer to DRAM will be generated any time the operand size is larger than the DRAM bank port size (e.g., line transfer to a 32-bit port, longword transfer to an 8-bit port). After completing the burst transfer, the MCF5206 negates $\overline{RAS}$, closing the page. Because all secondary transfers of a burst are guaranteed to be page hits, a page miss will never occur in burst page mode. Nonburst transfers will occur as in normal mode (for nonburst transfers in burst page mode, refer to **Section 10.3.8.1 Alternate Master NonBurst Transfer in Normal Mode**). Therefore, burst page mode will always give the same or better performance than normal mode.

Because the DRAMC does not support fast page mode for alternate master transfers, a DRAM bank programmed for either burst page mode or fast page mode will operate as burst page mode.

The timing of read transfers and write transfers is identical in burst page mode, with the exception of when the DRAM drives data on reads and when the alternate master drives data on writes.

The fastest possible alternate master burst transfer in burst page mode requires 5 clocks for the first transfer of the burst and two clocks for the secondary transfers. The fastest

possible nonburst transfer in burst page mode requires 5 clocks. You can program the DCTR to generate slower burst-page-mode transfers.

Figure 10-16 illustrates the timing of a word read transfer to an 8-bit DRAM in burst page mode. In burst page mode after the first byte transfer of the burst is complete, $\overline{RAS}$ remains asserted while $\overline{CAS}$[0] and $\overline{TA}$ are negated and the column address of the second byte transfer of the burst is driven. After the $\overline{CAS}$ precharge time is met, $\overline{CAS}$[0] asserts for the second byte read transfer. When the second byte read transfer is completed, $\overline{RAS}$, $\overline{CAS}$[0], and $\overline{TA}$ are negated, ending the burst transfer.

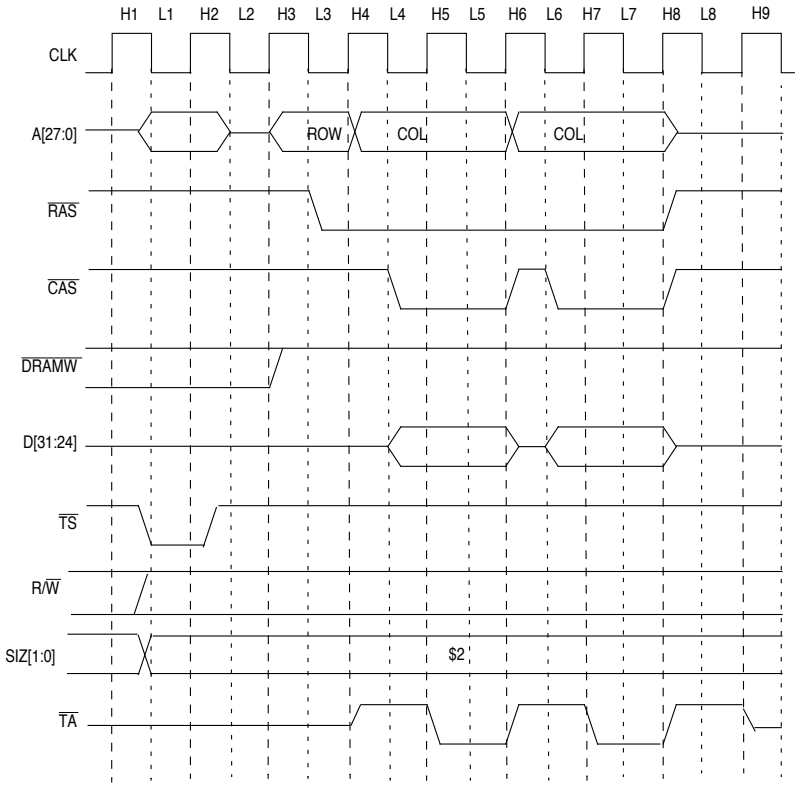

Figure 10-16. Alternate Master Word Read Transfer in Burst Page Mode with 8-Bit DRAM

Clock H1/L1

An alternate master is the current bus master. The alternate master starts a DRAM burst word-write transfer by driving A[27:0], driving R/$\overline{W}$ high indicating a read transfer, driving

$\overline{SIZ}$[1:0] to $2 indicating a word transfer, and asserting $\overline{TS}$. These inputs to the MCF5206 must be set up with respect to the rising edge of CLK H2.

Clock H2

On the rising edge of CLK when $\overline{TS}$ is asserted, the MCF5206 registers the address and attribute signals. It will internally decode these signals and determine if the alternate master transfer is a DRAM access. The alternate master negates $\overline{TS}$ and must three-state A[27:0] after the rising edge of CLK H2, if the internal address multiplexing is to be used.

Clock H3

The MCF5206 has determined that the alternate master transfer is a DRAM access, so the MCF5206 drives A[27:0] with the same value as was registered on the rising edge of H2. A[27:9] will be the DRAM row address. The MCF5206 also drives $\overline{DRAMW}$ high indicating a DRAM read cycle.

Clock L3

The MCF5206 asserts $\overline{RAS}$ to indicate the row address is valid on A[27:9].

Clock H4

The MCF5206 internally multiplexes the address and drives out the column address on A[27:9]. The MCF5206 also actively drives $\overline{TA}$ negated.

Clock L4

The MCF5206 asserts $\overline{CAS}$[0] to indicate the column address is valid on A[27:9]. At this point the DRAM will turn on it's output drivers and begin driving the data on D[31:24].

Clock H5

The MCF5206 asserts the $\overline{TA}$ signal to indicate that the first byte read transfer of the burst will be completed and the read data will be valid on D[31:24] on the next rising edge of CLK.

Clock H6

The MCF5206 negates $\overline{CAS}$[0], and $\overline{TA}$, ending the first byte read transfer of the burst. Because the bank is in burst page mode, the MCF5206 continues to assert $\overline{RAS}$. The negation of $\overline{CAS}$[0] starts the $\overline{CAS}$ precharge. The MCF5206 drives the column address on A[27:9] for second byte read transfer of the burst.

Clock L6

After the $\overline{CAS}$ precharge time is met, the MCF5206 asserts $\overline{CAS}$[0] to indicate the column address is valid on A[27:9]. At this point the DRAM will turn on its output drivers and begin driving the data bus.

Clock H7

Clock H7 is the same as Clock H5.

Clock H8

The MCF5206 negates $\overline{RAS}$, $\overline{CAS}$[0], and $\overline{TA}$, and three-states A[27:0], ending the final byte read transfer of the burst. Because the bank is in burst page mode, MCF5206 negates $\overline{RAS}$ when the burst transfer is completed. The negation of $\overline{RAS}$ starts the $\overline{RAS}$ precharge. Once A[27:0] has three-stated, the alternate master can start another transfer.

Clock H9

The MCF5206 three-states $\overline{TA}$.

10.3.8.4 LIMITATIONS. Because the external and internal address buses differ in size and address multiplexing occurs for transfers to DRAM, certain limitations exist for alternate master use of the DRAMC.

- Fast page mode is not available for alternate master transfers. If a bank has this featured enabled, then burst page mode will be used for alternate master transfers and fast page mode will be used for ColdFire core-initiated transfers.
- The UC, UD, SC, and SD mask bits are ignored during alternate master-initiated transfers. Therefore, if UC, UD, SC, and SD are all masked, that bank will be available for alternate master transfers even though the bank is unavailable for ColdFire core-initiated transfers.
- In determining whether an alternate master transfer address hits in a DRAM bank, the bits of the internal address bus which is unavailable externally will be regarded as “0's.” A[31:28] will always be set to 0 and A[27:24] will conditionally (based on PAR) be set to 0. In order for a bank to be accessible for alternate-master transfers, the address bits that are unavailable to the alternate master must either be set to 0 in the DCAR or be masked in the DCMR.
- DRAM bank size is limited by the availability of A[27:24] as determined by the PAR control register.

10.4 PROGRAMMING MODEL

10.4.1 DRAM Controller Registers Memory Map

Table 10-10 shows the memory map of all the DRAMC registers. The internal registers in the DRAM controller are memory-mapped registers offset from the MBAR address pointer.

The following lists several key notes regarding the programming model table:

- Addresses not assigned to a register and undefined register bits are reserved for future expansion. Write accesses to these reserved address spaces and reserved register bits have no effect; read accesses will return zeros.
- The reset value column indicates the register initial value at master reset and normal reset. Certain registers are uninitialized upon reset—they may contain random values after reset.
- The access column indicates if the corresponding register allows both read/write functionality (R/W), read-only functionality (R), or write-only functionality (W). If a read access to a write-only register is attempted, zeros will be returned. If a write access to a read-only register is attempted, the access will be ignored and no write will occur.

Table 10-10. Memory Map of DRAM Controller Registers

ADDRESS	NAME	WIDTH	DESCRIPTION	RESET VALUE	ACCESS
MBAR + $46	DCRR	16	DRAM Controller Refresh	Master Reset: $0000 Normal Reset: uninitialized	R/W
MBAR + $4A	DCTR	16	DRAM Controller Timing Register	Master Reset: $0000 Normal Reset: uninitialized	R/W
MBAR + $4C	DCAR0	16	DRAM Controller Address Register - Bank 0	Master Reset: uninitialized Normal Reset: uninitialized	R/W
MBAR + $50	DCMR0	32	DRAM Controller Mask Register - Bank 0	Master Reset: uninitialized Normal Reset: uninitialized	R/W
MBAR + $57	DCCR0	8	DRAM Controller Control Register- Bank 0	Master Reset: $00 Normal Reset: $00	R/W
MBAR + $58	DCAR1	16	DRAM Controller Address Register - Bank 1	Master Reset: uninitialized Normal Reset: uninitialized	R/W
MBAR + $5C	DCMR1	32	DRAM Controller Mask Register - Bank 1	Master Reset: uninitialized Normal Reset: uninitialized	R/W
MBAR + $63	DCCR1	8	DRAM Controller Control Register - Bank 1	Master Reset: $00 Normal Reset: $00	R/W

10.4.2 DRAM Controller Registers

10.4.2.1 DRAM CONTROLLER REFRESH REGISTER (DCRR). The DRAM Controller Refresh Register (DCRR) controls the number of system clocks between refresh cycles. The DCRR is a 16-bit read/write control register. The DCRR is set to $0000 by master reset (corresponding to the slowest refresh rate) and is unaffected by normal reset.

DRAM Controller Refresh Counter(DCRR) — Address MBAR + $46

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	RC11	RC10	RC9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
MASTER RESET: 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NORMAL RESET: 0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-

RC11 - RC0 - Refresh Count

This field controls the frequency of refresh requests. The value stored in this field is multiplied by 16 system clocks to determine the refresh period. The refresh period can range from 16 system clocks to 65,536 system clocks. An RC field value of all zeros corresponds to 65,536 system clocks. Any write to the DCRR will force a refresh cycle to occur. The refresh period can be calculated using the following equations:

For RC>$000:

Refresh period = RC x16 x (1/system clock frequency)

For RC=$000:

Refresh period = 65536 x (1/system clock frequency)

10.4.2.2 DRAM CONTROLLER TIMING REGISTER (DCTR). The DCTR controls the waveform timing for all DRAM transfers. The fields in this register control the $\overline{RAS}$ and $\overline{CAS}$ waveform timing for all types of DRAM transfers provided by the DRAMC. The DCTR is a 16-bit read/write control register. The DCTR is set to $0000 by master reset and is unaffected by normal reset.

DRAM Controller Timing Register(DCTR) — Address MBAR + $4A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAEM	EDO	-	RCD	-	RSH1	RSH0	-	-	RP1	RP0	-	CAS	-	CP	CSR
MASTER RESET: 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NORMAL RESET: -	-	0	-	0	-	-	0	0	-	-	0	-	0	-	-

DAEM - Drive Multiplexed Address During Alternate Master DRAM transfers

This field controls the MCF5206 output driver enables for the external address bus during alternate master transfers that hit in DRAM address space. If DAEM is set to 1, the portion of A[27]/$\overline{CS}$[7]/$\overline{WE}$[0], A[26]/$\overline{CS}$[6]/$\overline{WE}$[1], A[25]/$\overline{CS}$[5]/$\overline{WE}$[2], A[24]/$\overline{CS}$[4]/$\overline{WE}$[3] that are configured as address signals will be driven along with A[23:0] to provide row and column address multiplexing for alternate masters. This field does not affect the address multiplexing for DRAM transfers initiated by the ColdFire core.

0 = Do not drive the external address signals as outputs during alternate master DRAM transfers
1 = Drive the external address signals as outputs to provide row and column address multiplexing during alternate master DRAM transfers

EDO - Extended Data-Out Enable

This field controls page mode $\overline{CAS}$ timing. If the DRAM banks are populated with extended data-out DRAM, the EDO Enable bit can be set to take advantage of the $\overline{CAS}$ timing allowed by EDO DRAMs. The EDO Enable bit, along with the CAS and CP bits,

control the $\overline{CAS}$ assertion and negation time during fast page mode and burst page mode transfers. Refer to Figure 10-21 for a timing diagram of EDO DRAM page mode transfers.

0 = DRAM banks are populated with standard DRAM, do not use EDO $\overline{CAS}$ timing
1 = DRAM banks are populated with EDO DRAM, use EDO $\overline{CAS}$ timing

NOTE

If neither fast page mode or burst page mode are enabled in the DRAM Control Register (DCCR), the EDO Enable bit has no affect on the DRAM waveform timing.

RCD - $\overline{RAS}$-to-$\overline{CAS}$ Delay Time

This field controls the number of system clocks between the assertion of $\overline{RAS}$ and the assertion of $\overline{CAS}$ for transfers in normal mode and for the initial transfer to a page in fast page mode and burst page mode. Because the column address is always driven 0.5 system clocks prior to the assertion of $\overline{CAS}$, RCD affects the driving of the column address. RCD does not affect refresh cycles. Refer to Figure 10-17 for normal mode timing. Refer to Figure 10-18 and Figure 10-19 for fast page mode and burst page mode timing.

0 = $\overline{RAS}$ will assert 1.0 system clock before the assertion of $\overline{CAS}$
1 = $\overline{RAS}$ will assert 2.0 system clocks before the assertion of $\overline{CAS}$

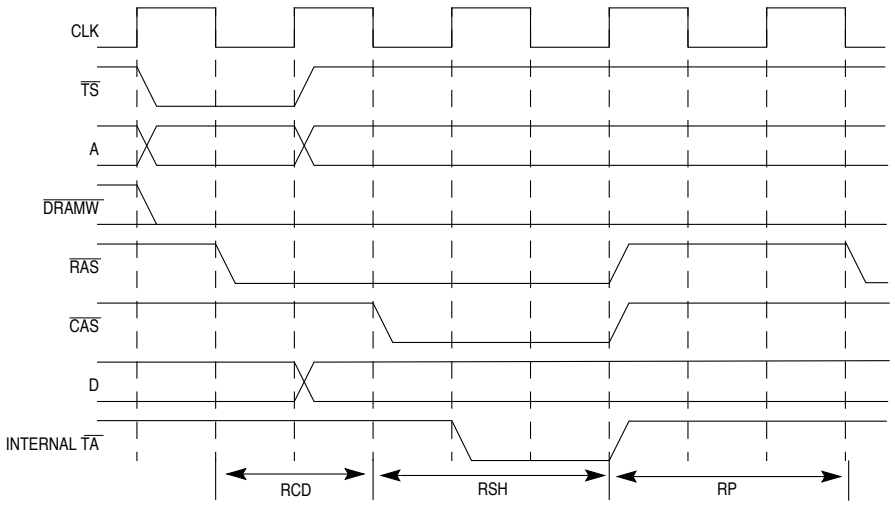

Figure 10-17. Normal Mode DRAM Transfer Timing

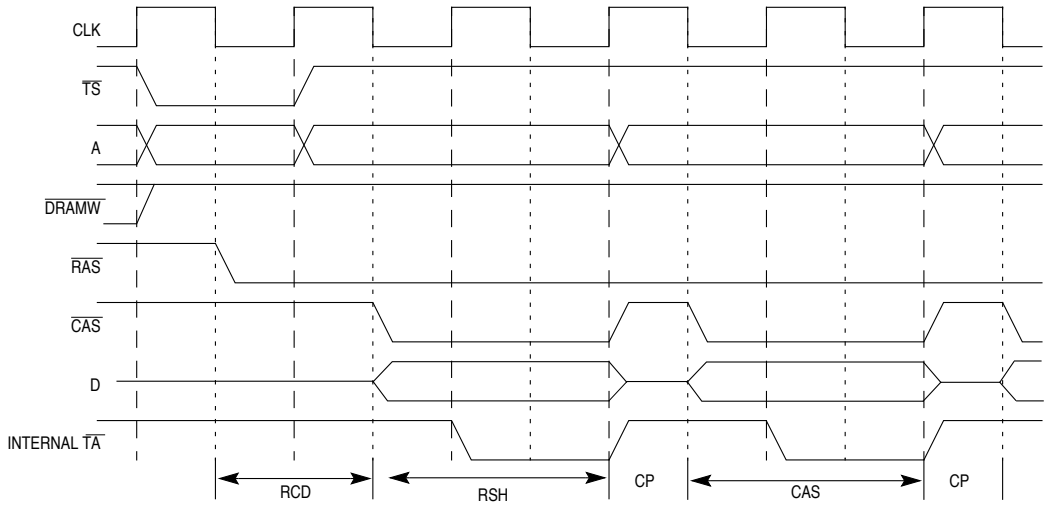

Figure 10-18. Fast Page Mode or Burst Page Mode DRAM Transfer Timing

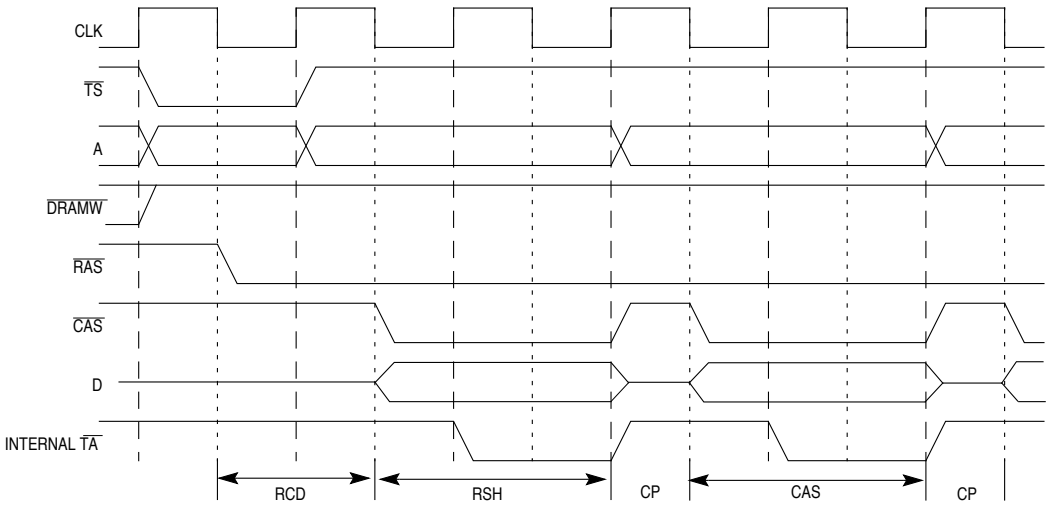

Figure 10-19. Fast Page Mode or Burst Page Mode DRAM Transfer Timing

RSH1 - RSH0 - $\overline{RAS}$ Hold Time

This field controls the number of system clocks that $\overline{RAS}$ will remain asserted after the assertion of $\overline{CAS}$. This field controls $\overline{RAS}$ active timing for transfers in normal mode and for the initial transfer in fast page mode and burst page mode. Refer to Figure 10-17 for

normal mode timing. Refer to Figure 10-19 and Figure 10-21 for fast-page-mode and burst- page-mode timing.

For transfers in normal mode:

00 = $\overline{RAS}$ will negate 1.5 system clocks after the assertion of $\overline{CAS}$
01 = $\overline{RAS}$ will negate 2.5 system clocks after the assertion of $\overline{CAS}$
10 = $\overline{RAS}$ will negate 3.5 system clocks after the assertion of $\overline{CAS}$
11 = Reserved

For the initial transfer in fast page mode and burst page mode with EDO Enable = 0:

00 = $\overline{RAS}$ will negate 1.5 system clocks after the assertion of $\overline{CAS}$
01 = $\overline{RAS}$ will negate 2.5 system clocks after the assertion of $\overline{CAS}$
10 = $\overline{RAS}$ will negate 3.5 system clocks after the assertion of $\overline{CAS}$
11 = Reserved

For initial transfer in fast page mode and burst page mode with EDO Enable = 1:

00 = $\overline{RAS}$ will negate 1.0 system clocks after the assertion of $\overline{CAS}$
01 = $\overline{RAS}$ will negate 2.0 system clocks after the assertion of $\overline{CAS}$
10 = $\overline{RAS}$ will negate 3.0 system clocks after the assertion of $\overline{CAS}$
11 = Reserved

RP1 - RP0 - $\overline{RAS}$ Precharge Time

This field controls the number of system clocks $\overline{RAS}$ will precharge when the bus master requires back-to-back DRAM transfers in normal mode. RP also controls the number system clocks $\overline{RAS}$ will precharge after a refresh cycle or when a page is closed in fast page mode or burst page mode. Refer to Figure 10-22 for refresh cycle timing. Refer to Figure 10-17 for normal mode timing. Refer to Figure 10-20 for fast page-mode timing.

00 = $\overline{RAS}$ will precharge for 1.5 system clocks
01 = $\overline{RAS}$ will precharge for 2.5 system clocks
10 = $\overline{RAS}$ will precharge for 3.5 system clocks
11 = Reserved

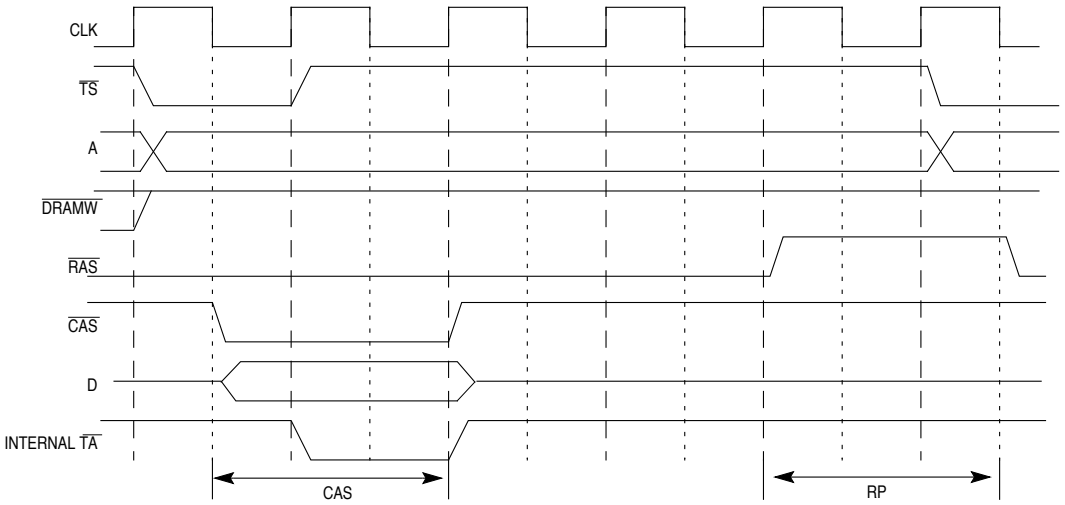

Figure 10-20. Fast Page Mode Page Hit and Page Miss DRAM Transfer Timing

CAS - Column Address Strobe Time

This field, together with the EDO field, controls the number of system clocks that $\overline{CAS}$ will be asserted on transfers once a page is open in fast page mode and burst page mode. Refer to Figure 10-18 for timing diagrams of fast-page-mode or burst-page- mode transfers to standard DRAMs and Figure 10-21 for fast-page-mode or burst-page-mode transfers to EDO DRAMs.

For EDO = 0:

0 = $\overline{CAS}$ will be asserted for 1.5 system clocks
1 = $\overline{CAS}$ will be asserted for 2.5 system clocks

For EDO = 1:

0 = $\overline{CAS}$ will be asserted for 1.0 system clocks
1 = $\overline{CAS}$ will be asserted for 2.0 system clocks

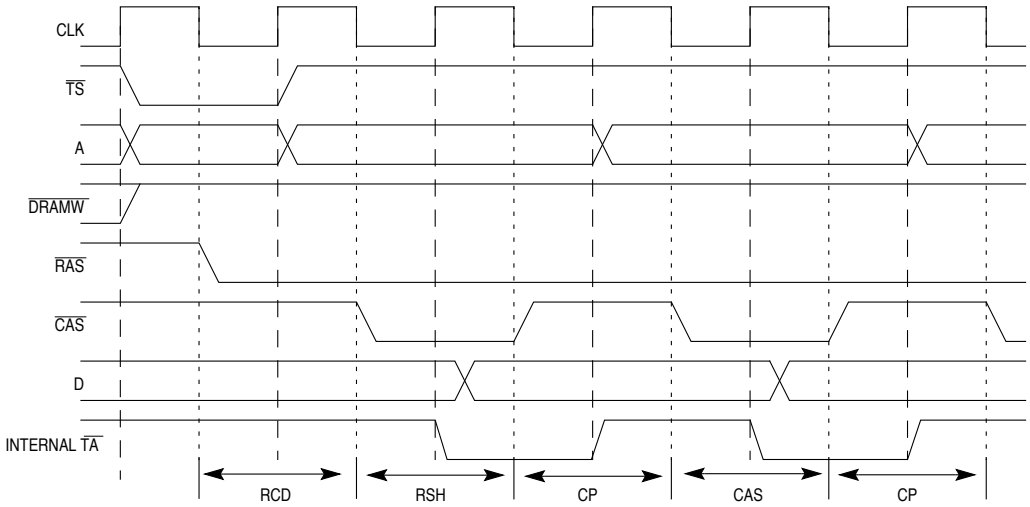

Figure 10-21. Fast Page Mode or Burst Page Mode EDO DRAM Transfer Timing

CP - $\overline{\text{CAS}}$ Precharge Time

This field, together with the EDO field, controls the number of system clocks that $\overline{\text{CAS}}$ will be negated after a page mode transfer. This field controls $\overline{\text{CAS}}$ timing for fast page mode and burst page mode. Refer to Figure 10-6 and Figure 10-7 for timing diagrams illustrating $\overline{\text{CAS}}$ precharge timing in fast page mode and burst page mode using standard and EDO DRAMs.

For EDO Enable = 0:

0 = $\overline{\text{CAS}}$ will be negated for 0.5 system clocks
1 = CAS will be negated for 1.5 system clocks

For EDO Enable = 1:

0 = $\overline{\text{CAS}}$ will be negated for 1.0 system clocks
1 = CAS will be negated for 2.0 system clocks

CSR - $\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

This field controls the number of system clocks between the assertion of $\overline{\text{CAS}}$ and the assertion of $\overline{\text{RAS}}$ during refresh cycles. This field does not affect normal mode, fast page mode, or burst-page-mode transfer timing. Refer to Figure 10-22 for refresh cycle timing.

0 = $\overline{\text{CAS}}$ will assert 1.0 system clock before the assertion of $\overline{\text{RAS}}$
1 = $\overline{\text{CAS}}$ will assert 2.0 system clocks before the assertion of $\overline{\text{RAS}}$

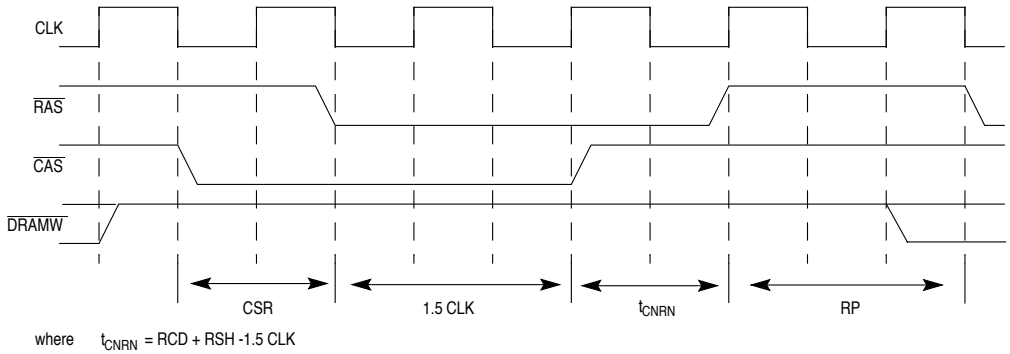

Figure 10-22. CAS Before RAS Refresh Cycle Timing

NOTE

The DCTR should not be written while an alternate master transfer is in progress. It should be programmed as part of the initialization sequence and alternate master DRAM transfers should not be attempted until it has been written. Failure to do so will result in unpredictable operation.

10.4.2.3 DRAM CONTROLLER ADDRESS REGISTERS (DCAR0 - DCAR1). Each DCAR holds the base address of the corresponding DRAM bank. Each DCAR is a 16-bit read/write control register. All bits in DCAR0 - DCAR1 are unaffected by either master reset or normal reset.

DRAM Controller Address Register(DCAR)

Address MBAR + $4C (Bank0)
Address MBAR + $58 (Bank1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BA31	BA30	BA29	BA28	BA27	BA26	BA25	BA24	BA23	BA22	BA21	BA20	BA19	BA18	BA17	-
NORMAL OR MASTER RESET:															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0

BA31-BA17 - Base Address

This field defines the base address location of each DRAM bank. These bits are compared to bits 31-17 of the transfer address to determine if the DRAM bank is being accessed.

NOTE

In determining whether an alternate master transfer address hits in a DRAM bank, the portion of the address bus that is unavailable externally will be regarded as “0's.” That is, the alternate master transfer address will always have A[31:28] as 0’s and those bits of A[27:24] that are not programmed to be

external address bits as 0's. In order for a bank to be accessible to an alternate master, the address bits that are unavailable to the alternate master must either be set to 0 in the DCAR or be masked in the DCMR.

10.4.2.4 DRAM CONTROLLER MASK REGISTER (DCMR0 - DCMR1). Each DCMR holds the address mask for each of the DRAM banks as well the definition of which types of transfers are allowed for the DRAM banks. Each DCMR is a 32-bit read/write control register. All bits in DCMR0 - DCMR1 are unaffected by either Master Reset or normal reset.

DRAM Controller Mask Register(DCMR)

Address MBAR + $50 (Bank0)
Address MBAR + $5C (Bank1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BAM31	BAM30	BAM29	BAM28	BAM27	BAM26	BAM25	BAM24	BAM23	BAM22	BAM21	BAM20	BAM19	BAM18	BAM17	-
NORMAL OR MASTER RESET:															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	SC	SD	UC	UD	-
NORMAL OR MASTER RESET:															
0	0	0	0	0	0	0	0	0	0	0	-	-	-	-	0

BAM31-BAM17 - Base Address Mask

This field defines the DRAM address space through the use of address mask bits. Any bit set to 1 masks the corresponding base address register (DCAR) bit (the base address bit becomes a ‘‘don’t care’’ in the address comparison). Unmasked base address bits are compared to the ColdFire core or alternate master transfer address to determine if the transfer is accessing a DRAM address space.

0 = Corresponding address bit is used in DRAM bank decode
1 = Corresponding address bit is a ‘‘don’t care’’ in DRAM bank decode

SC, SD, UC, UD - Supervisor Code, Supervisor Data, User Code, User Data Transfer Mask

This field masks allows specific types of transfers to be inhibited from accessing the DRAM bank. If a transfer mask bit is cleared, a transfer of that type can access the corresponding DRAM bank. If a transfer mask bit is set to 1, an transfer of that type can not access the corresponding DRAM bank. The transfer mask bits are:

SC = Supervisor Code mask
SD = Supervisor Data mask
UC = User Code mask
UD = User Data mask

For each transfer mask bit:

0 = Do not mask this type of transfer for the DRAM bank. A transfer of this type can access the DRAM bank
1 = Mask this type of transfer for the DRAM bank. A transfer of this type cannot access the DRAM bank

NOTE

The SC, SD, UC, and UD bits are ignored during alternate master transfers. Therefore, an alternate master transfer can access the DRAM banks regardless of the transfer masks.

NOTE

In determining whether an alternate master transfer address hits in a DRAM bank, the portion of the address bus that is unavailable externally will be regarded as “0's.” That is, the alternate master transfer address will always have A[31:28] as 0’s and those bits of A[27:24] that are not programmed to be external address bits as 0’s. In order for a bank to be accessible to an alternate master, the address bits that are unavailable to the alternate master must either be set to 0 in the DCAR or be masked in the DCMR.

10.4.2.5 DRAM CONTROLLER CONTROL REGISTER (DCCR0 - DCCR1). Each DCCR specifies the port size, page size, page mode, and activation of each of the DRAM banks. Each DCCR is an 8-bit read/write control register. Master reset and normal reset set all bits to zero.

DRAM Controller Control Register(DCCR) — Address MBAR + $57 (Bank0), Address MBAR + $63 (Bank1)

7	6	5	4	3	2	1	0
PS1	PS0	BPS1	BPS0	PM1	PM0	WR	RD
NORMAL OR MASTER RESET: 0	0	0	0	0	0	0	0

PS - Port Size

This field specifies the data width of the DRAM bank. PS determines the byte lanes that data will be driven on during write cycles and the byte lanes that data will be sampled from during read cycles.

00 = 32-bit port size - Data sampled and driven on D[31:0]
01 = 8-bit port size - Data sampled and driven on D[31:24] only
10 = 16-bit port size - Data sampled and driven on D[31:16] only
11 = 16-bit port size - Data sampled and driven on D[31:16] only

BPS - Bank Page Size

This field defines the bank page size for each DRAM bank for fast page mode and burst page mode.

00 = 512 byte page size
01 = 1 kbyte page size
10 = 2 kbyte page size
11 = Reserved

PM - Page Mode Select

This field selects the type of DRAM transfers generated for each DRAM bank: normal mode, fast page mode, or burst-page-mode transfers.

00 = Normal Mode
01 = Burst Page Mode
10 = Reserved
11 = Fast Page Mode

WR - Write Enable

This field controls whether the DRAM bank can be accessed during write transfers.

0 = Do not activate DRAM control signals on write transfers
1 = Activate DRAM control signals on write transfers

RD - Read Enable

This field controls whether the DRAM bank can be accessed during read transfers.

0 = Do not activate DRAM control signals on read transfers
1 = Activate DRAM control signals on read transfers

10.5 DRAM INITIALIZATION EXAMPLE

The following sample of assembly program illustrates a DRAM initialization procedure. DRAM bank 0 is configured for a 4 Mbyte DRAM starting at address 0x00100000. The DRAM port size is programmed to 32-bit (1 Mbyte x 32), the page size to 512 byte, and fast page mode is enabled.

The Module Base Address Register (MBAR) is first written with the MODULE_BASE value. This locates all the MCF5206 internal modules at address 0x00004000. Then the DRAM Controller Timing Register (DCTR) is initialized to give the fastest possible DRAM transfer waveform timing. The DRAM Controller Refresh Register (DCRR) is then written causing DRAM refresh cycles to be generated once every 512 clocks (15.4 μsec for a 33 MHz system clock). Once the DCRR is written, a refresh cycle is immediately generated and refresh cycles start being generated at the newly programmed rate. Next, DRAM Controller Address Register 0 (DCAR0) is written, making the starting address of DRAM bank 0 0x00100000. DRAM Controller Mask Register 0 (DCMR0) is then written such that transfer address bits 18 - 16 are masked, making the DRAM bank 0 address space 1

Mbyte. Therefore, DRAM bank 0 address space ranges from 0x00100000 - 0x001EFFFF. DRAM Controller Control Register 0 (DCCR0) is then written making DRAM bank 0 have a 32-bit port size, a 512 byte bank page size, generate fast-page-mode transfers, and be enabled for both read transfers and write transfers. At this point, DRAM bank 0 is initialized; however, DRAM read and write transfers will not be generated until the global chip-select is disabled by writing CSMR0.

```
# set up variables

MODULE_BASE equ 0x00004001  Base address of internal module registers
DRAM0_BASE equ 0x0010       Base address for Bank0 DRAM
DCRRequ 0x46                DRAMC Refresh Register
DCTRequ 0x4a                DRAMC Timing Register
DCAR0equ 0x4c               DRAMC Address Register 0
DCMR0equ 0x50               DRAMC Mask Register 0
DCCR0equ 0x57               DRAMC Control Register 0
CSMR0equ 0x68               Chip-select Mask Register 0

# DRAMC initialization

move.l  #MODULE_BASE, d0    Initialize MBAR
movec  d0, mbar
move.l #MODULE_BASE, a0     a0 points to the module base address

move.w #0x00, d0            Initialize for fastest DRAM cycle timing
move.w d0, (DCTR, a0)       (RCD=RSH1=RSH0=RP1=RP0=CAS=CP=CSR=0)

move.w #0x20, d0            Refresh every 512 clocks (15.4 uS @ 33Mhz)
move.w d0, (DCRR, a0)

move.w #DRAM0_BASE, d0      Set DRAM0 start address at 0x00100000
move.w d0, (DCAR0, a0)

move.l #0x000e0000, d0      Mask low order bits for 1Mbyte address space
move.l d0, (DCMR0, a0)      DRAM0 address space is 0x0010-0x001effff

move.b #0x0f, d0            32-bit port, 512-byte page, fast page mode,
move.b d0, (DCCR0, a0)      Readable/writable

# The global chip-select activates for ALL external transfers after reset until
it is disabled. Therefore, before a DRAM transfer can be done, the global chip
select must be disabled by writing CSMR0.
```