# SECTION 13
# TIMER MODULE

## 13.1 OVERVIEW OF THE TIMER MODULE

The MCF5206 contains two general-purpose16-bit timers. This section of the manual documents how the 16-bit timer operates.

The output of an 8-bit prescaler clocks each 16-bit timer. The prescaler input can be the system clock, the system clock divided by 16, or the timer input (TIN) pin. Figure 13-1 is a block diagram of the Timer module.

## 13.2 OVERVIEW OF KEY FEATURES

The general-purpose 16-bit timer unit has the following features:

- Maximum period of 8 seconds at 33 MHz, 11 seconds at 25 MHz, and 16 seconds at 16.67 MHz
- 30 ns resolution at 33 MHz, 40 ns at 25 MHz, 60 ns at 16.67 MHz
- Programmable sources for the clock input, including external clock
- Input-capture capability with programmable trigger edge on input pin
- Output-compare with programmable mode for the output pin
- Free run and restart modes
- Maskable interrupts on input capture or reference-compare

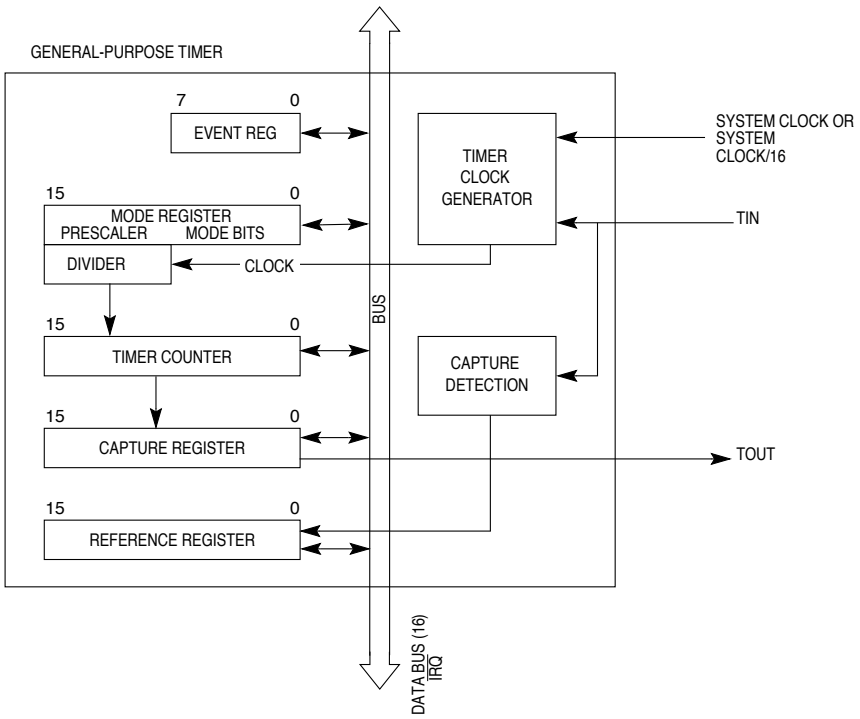



**Figure 13-1. Timer Block Diagram Module Operation**

## 13.3 UNDERSTANDING THE GENERAL-PURPOSE TIMER UNITS

The general-purpose timer units provide the following features:

- You can program timers to count and compare to a reference value stored in a register or capture the timer value at an edge detected on the TIN pin
- An 8-bit prescalar output clocks the timers
- You can program the prescalar clock input
- Programmed events generate interrupts
- You can configure the TOUT pin to toggle or pulse on an event

The maximum resolution of each timer is one system clock cycle (30 ns at 33 MHz). To obtain the maximum period, divide the system clock by 16, set the prescaler value to divide by 256, and load the reference value with ones. This maximum period is 268,435,456 cycles (8.05 seconds at 33 MHz).

### 13.3.1 Selecting the Prescaler

You can select the prescalar clock from the main clock (divided by 1 or by 16) or from the corresponding timer input TIN pin. TIN is synchronized to the internal clock. The synchronization delay is between two and three main clocks. TIN must meet the setup time spec shown in the AC Electrical Specs section.

The ICLK bits of the corresponding Timer Mode Register (TMR) select the clock input source. The prescaler is programmed to divide the clock input by values from 1 to 256. The prescalar output is used as an input to the 16-bit counter.

### 13.3.2 Working with Capture Mode

The timer has a 16-bit Timer Capture Register (TCR) that latches the counter value when the corresponding input capture-edge detector senses a defined transition (of TIN). The capture edge (CE) bits in the TMR select the type of transition triggering the capture. A capture event sets the Timer Event Register (TER) bit and issues a maskable interrupt.

### 13.3.3 Configuring the Timer for Reference Compare

You can configure the timer to count until it reaches a reference value at which time it either starts a new time count immediately or continues to run. The free run/restart (FRR) bit of the TMR selects either mode. When the timer reaches the reference value, the TER bit is set and issues an interrupt if the output reference interrupt (ORI) enable bit in TMR is set.

### 13.3.4 Configuring the Timer for Output Mode

The timer can send an output signal on the timer output (TOUT) pin when it reaches the reference value as selected by the output mode (OM) bit in the TMR. This signal can be an active-low pulse or a toggle of the current output under program control.

## 13.4 PROGRAMMING MODEL

### 13.4.1 Understanding the General-Purpose Timer Registers

You can modify the timer registers at any time. Table 13-1 illustrates the programming model.

**Table 13-1. Programming Model for Timers**

| TIMER 1 ADDRESS | TIMER 2 ADDRESS | SIM MODULE–TIMER MODULE REGISTERS | |
|---|---|---|---|
| MBAR+$100 | MBAR+$120 | Timer Mode Register (TMR) | |
| MBAR+$104 | MBAR+$124 | Timer Reference Register (TRR) | |
| MBAR+$108 | MBAR+$128 | Timer Capture Register (TCR) | |
| MBAR+$10C | MBAR+$12C | Timer Counter (TCN) | |
| MBAR+$111 | MBAR+$131 | Reserved | Timer Event Register (TER) |

**13.4.1.1 TIMER MODE REGISTER (TMR).** TMR is a 16-bit memory-mapped register. This register programs the various timer modes and is cleared by reset.

Timer Mode Register (TMR) — Address MBAR+$100, MBAR+$120

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PRESCALER VALUE (PS7 - PS0) | | | | | | | | CE1-CE0 | | OM | ORI | FRR | ICLK1-ICLK0 | | RST |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Read/Write — Supervisor or User Mode

PS7–PS0 — Prescaler Value

The prescaler is programmed to divide the clock input by values from 1 to 256. The value 00000000 divides the clock by 1; the value 11111111 divides the clock by 256.

CE1–CE0 — Capture Edge and Enable Interrupt

- 11 = Capture on any edge and enable interrupt on capture event
- 10 = Capture on falling edge only and enable interrupt on capture event
- 01 = Capture on rising edge only and enable interrupt on capture event
- 00 = Disable interrupt on capture event

OM — Output Mode

- 1 = Toggle output
- 0 = Active-low pulse for one system clock cycle (30ns at 33 MHz)

ORI — Output Reference Interrupt Enable

- 1 = Enable interrupt upon reaching the reference value
- 0 = Disable interrupt for reference reached (does not affect interrupt on capture function)

**NOTE**

If ORI is set when the REF event is asserted in the Timer Event Register (TER), an immediate interrupt will occur. If ORI is cleared while an interrupt is asserted, the interrupt will negate.

FRR — Free Run/Restart

- 1 = Restart: Timer count is reset immediately after reaching the reference value
- 0 = Free run: Timer count continues to increment after reaching the reference value

CLK1–CLK0 — Input Clock Source for the Timer

- 11 = TIN pin (falling edge)
- 10 = Master system clock divided by 16. Note that this clock source is not synchronized to the timer; thus successive time-outs may vary slightly in length
- 01 = Master system clock
- 00 = Stops counter. After the counter is stopped, the value in the Timer Counter (TCN) register will remain constant.

RST — Reset Timer

This bit performs a software timer reset identical to that of an external reset. All timer registers will take on their corresponding reset values. While this bit is zero, the other register values can still be written, if necessary. A transition of this bit from one to zero is what resets the register values. The counter/timer/prescaler will not be clocked unless the timer is enabled.

1 = Enable timer
0 = Reset timer (software reset)

**13.4.1.2 TIMER REFERENCE REGISTER (TRR).** The TRR is a 16-bit register containing the reference value that is compared with the free-running timer counter (TCN) as part of the output-compare function. TRR is a memory-mapped read/write register.

TRR is set at reset. The reference value is not matched until TCN equals TRR, and the prescaler indicates that the TCN should be incremented again. Thus, the reference register is matched after (TRR+1) time intervals.

Timer Reference Register (TRR) — Address MBAR+$104,MBAR+$124

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 16-BIT REFERENCE COMPARE VALUE REF15 - REF0 | | | | | | | | | | | | | | | |
| RESET | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Read/Write | | | | | | | | | | | | Supervisor or User Mode | | | |

**13.4.1.3 TIMER CAPTURE REGISTER (TCR).** The TCR is a 16-bit register that latches the value of the timer counter (TCN) during a capture operation when an edge occurs on the TIN pin, as programmed in the TMR. TCR appears as a memory-mapped read-only register to you and is cleared at reset.

Timer Capture Register (TCR) — Address MBAR+$108,MBAR+$128

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 16-BIT CAPTURE COUNTER VALUE CAP15 - CAP0 | | | | | | | | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read Only | | | | | | | | | | | | Supervisor or User Mode | | | |

**13.4.1.4 TIMER COUNTER (TCN).** TCN is a memory-mapped 16-bit up counter that you can read at any time. A read cycle to TCN yields the current timer value and does not affect the counting operation.

A write of any value to TCN causes it to reset to all zeros.

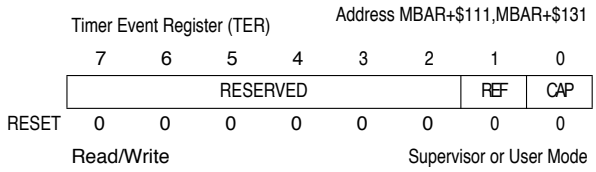
Timer Counter Register (TCN) — Address MBAR+$10C, MBAR+$12C

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 16-BIT TIMER COUNTER VALUE COUNT15 - COUNT0 | | | | | | | | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Read/Write | | | | | | | | | | | | Supervisor or User Mode | | | |

**13.4.1.5 TIMER EVENT REGISTER (TER).** The TER is an 8-bit register that reports events the timer recognizes. When the timer recognizes an event, it will set the appropriate bit in the TER, regardless of the corresponding interrupt-enable bits (ORI and CE) in the TMR.

TER, which appears to you as a memory-mapped register, can be read at any time.

You should write a one to a bit to clear it (writing a zero does not affect bit value); more than one bit can be cleared at a time. The REF and CAP bits must be cleared before the timer will negate the IRQ to the interrupt controller. Reset clears this register.




Bits 7–2 — Reserved for future use.

CAP — Capture Event

If a one is read from this bit, the counter value has been latched into the TCR. The CE bit in the TMR enables the interrupt request caused by this event. You should write a one to this bit to clear the event condition.

REF — Output Reference Event

If a one is read from this bit, the counter has reached the TRR value. The ORI bit in the TMR enables the interrupt request caused by this event. You should write a one to this bit to clear the event condition.