SECTION 16
ELECTRICAL CHARACTERISTICS

16.1 MAXIMUM RATINGS

16.1.1 Supply, Input Voltage and Storage Temperature

RATING	SYMBOL	VALUE	UNIT
Supply voltage	V_{DD}	-0.3 to +7.0	V
Input voltage	V_{in}	-0.5 to V_{DD} +0.5	V
Storage temperature range	T_{stg}	-55 to 150	°C

The ratings in the above table define maximum conditions under which the MCF5206 device may be subjected without being damaged. However, the device cannot operate normally while being exposed to these electrical extremes.

This device contains circuitry that protects against damage from high static voltages or electrical fields; however, you should take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Operational reliability improves when unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{DD}).

16.1.2 Operating Temperature

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Maximum operating junction temperature	T_J	TBD	°C
Maximum operating ambient temperature	T_{Amax}	70[a]	°C
Minimum operating ambient temperature	T_{Amin}	0	°C

[a] This published maximum operating ambient temperature should be used only as a system design guideline. All device operating parameters are guaranteed only when the junction temperature lies within the specified range.

NOTE

At press time power dissipation figures were not available. Refer to the World Wide Web site at http://www.mot.com/ColdFire for the latest accurate power dissipation information for the MCF5206 processor.

16.1.3 Thermal Resistance

CHARACTERISTIC	SYMBOL[b]	VALUE	RATING
Thermal resistance, junction to ambient Thermal resistance, junction to top reference	q_{ja} Y_{jt}	38 3	°C/W °C/W

[b] q_{ja} and Y_{jt} parameters are simulated in accordance with EIA/JESD Standard 51-2 for natural convection. Motorola recommends the use of q_{ja} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by the board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Y_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

16.1.4 Output Loading

CHARACTERISTIC	SYMBOL	MAXIMUM	UNIT
Load Capacitance (All signals)	C_L	50	pF

16.2 DC ELECTRICAL SPECIFICATIONS

CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
Operation voltage range	V_{DD}	4.75	5.25	V
Input high voltage	V_{IH}	2	V_{DD}	V
Input low voltage	V_{IL}	GND	0.8	V
Input signal undershoot	—	—	0.8	V
Input signal overshoot	—	—	0.8	V
Input leakage current @ GND, V_{DD} CLK, A[27:0], D[31:0], $\overline{TS}$, SIZ[1:0], R/$\overline{W}$, $\overline{TA}$, $\overline{ATA}$, $\overline{TEA}$, $\overline{IPL}$[2]/$\overline{IRQ}$[7], $\overline{IPL}$[1]/$\overline{IRQ}$[4], $\overline{IPL}$[0]/$\overline{IRQ}$[1], $\overline{BG}$, RxD[2:1], $\overline{CTS}$[2:1], TIN[1:0], PP[7:0]/PST[3:0]/DDATA[3:0], $\overline{RSTI}$, TCK, $\overline{HIZ}$, JTAG	I_{in}	—	20	uA
HI-Z (three-state) leakage current @GND, V_{DD} A[27:0], D[31:0], $\overline{TS}$, TT[1:0], ATM, SIZ[1:0], R/$\overline{W}$, $\overline{TA}$, TDO/DSO	I_{TSI}	—	20	uA
Signal Low Input Current, V_{IL} = 0.8V TMS/$\overline{BKPT}$, TDI/DSI, $\overline{TRST}$/DSCLK	I_{IL}	TBD	TBD	mA
Signal High Input Current, V_{IH} = 2.0V TMS/$\overline{BKPT}$, TDI/DSI, $\overline{TRST}$/DSCLK	I_{IH}	TBD	TBD	mA
Output high voltage, I_{OH} = 8mA (All signals except $\overline{RAS}$[1:0], $\overline{CAS}$[3:0], $\overline{DRAMW}$), I_{OH} = 16mA ($\overline{RAS}$[1:0], $\overline{CAS}$[3:0], $\overline{DRAMW}$)	V_{OH}	2.4	—	V
Output low voltage , I_{OL} = 8mA (All signals except $\overline{RAS}$[1:0], $\overline{CAS}$[3:0], $\overline{DRAMW}$), I_{OL} = 16mA ($\overline{RAS}$[1:0], $\overline{CAS}$[3:0], $\overline{DRAMW}$)	V_{OL}	—	0.5	V
Pin capacitance*	C_{in}	—	10	pF

* This specification periodically sampled but not 100% tested.

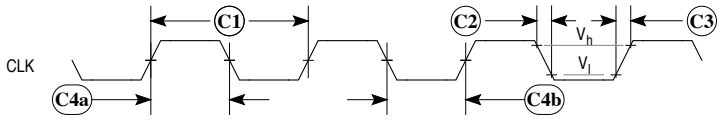
16.3 AC ELECTRICAL SPECIFICATIONS

16.3.1 Clock Input Timing Specifications

NAME	CHARACTERISTIC	16.67 MHz		25 MHz		33.33 MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
	Frequency of Operation[1]	0	16.67	0	25.00	0	33.33	MHz
C1	CLK cycle time	60	–	40	–	30	–	ns
C2[2]	CLK rise time (from V_l = 0.5V to V_h = 2.4V)	–	5	–	5	–	5	ns
C3[2]	CLK fall time(from V_h = 0.5V to V_l = 2.4V)	–	5	–	5	–	5	ns
C4	CLK duty cycle (measured at 1.5 V)	40	60	40	60	40	60	%
C4a[3]	CLK pulse width high (measured at 1.5 V)	24	36	16	24	12	18	ns
C4b[3]	CLK pulse width low (measured at 1.5 V)	24	36	16	24	12	18	ns

[1] CLK may be stopped to conserve power.
[2] Specification values are not tested.
[3] Specification values listed are for maximum frequency of operation.

16.3.2 Clock Input Timing Diagram

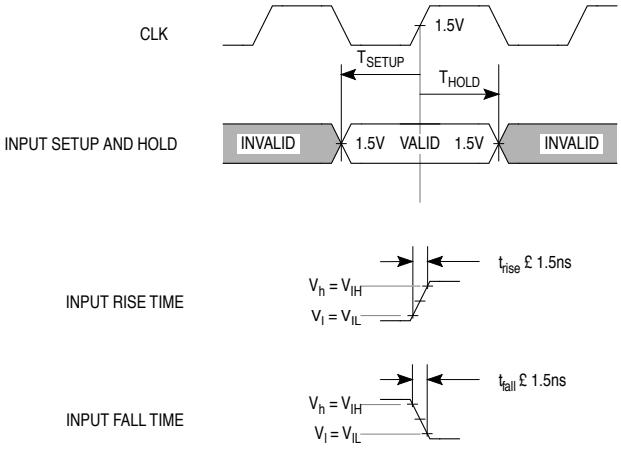


Clock Input Timing

16.3.3 Processor Bus Input Timing Specifications

NAME	CHARACTERISTIC	16.67 MHz		25 MHz		33.33 MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
CONTROL INPUTS								
B1a	$\overline{TS}$ Valid to CLK (Setup)	15	–	10	–	7	–	ns
B1b	$\overline{TA}$, Valid to CLK (Setup)	15	–	10	–	8	–	ns
B1c	$\overline{ATA}$ Valid to CLK (Setup)	3	–	3	–	2	–	ns
B1d	$\overline{TEA}$ Valid to CLK (Setup)	15	–	11	–	10	–	ns
B1e	$\overline{BG}$ Valid to CLK (Setup)	15	–	10	–	10	–	ns
B1f	$\overline{IPL}$[2:0]/$\overline{IRQ}$[7,4,1] Valid to CLK (Setup)	3	–	3	–	2	–	ns
B1g	$\overline{RSTI}$ Valid to CLK (Setup)	3	–	3	–	2	–	ns
B1h	DSCLK to CLK (Setup)	15	–	13	–	11	–	ns
B1i	$\overline{BKPT}$, DSI Valid to CLK (Setup)	15	–	10	–	7	–	ns
B2a	CLK to Synchronous Control Input ($\overline{TS}$, $\overline{TA}$, $\overline{TEA}$, $\overline{BG}$, DSI, DSCLK) Invalid (Hold)	3	–	3	–	2	–	ns
B2b	CLK to Asynchronous Control Input ($\overline{ATA}$, $\overline{IPL}$[2:0]/$\overline{IRQ}$[7,4,1], $\overline{RSTI}$, $\overline{BKPT}$) Invalid (Hold)	3	–	3	–	3	–	ns
B2c	CLK to Mode Selects Invalid ($\overline{RSTI}$ Asserted)	3	–	3	–	2	–	ns
ADDRESS AND ATTRIBUTE INPUTS								
B3	Address and Attribute Input (A[27:0], SIZ[1:0], R/$\overline{W}$) Valid to CLK (Setup)	15	–	10	–	7	–	ns
B4	CLK to Address and Attribute Input (A[27:0], SIZ[1:0], R/$\overline{W}$) Invalid (Hold)	3	–	3	–	2	–	ns
DATA INPUTS								
B5	Data Input (D[31:0]) Valid to CLK (Setup)	10	–	6	–	3	–	ns
B6	CLK to Data Input (D[31:0]) Invalid (Hold)	3	–	3	–	3	–	ns

16.3.4 Input Timing Waveform Diagram



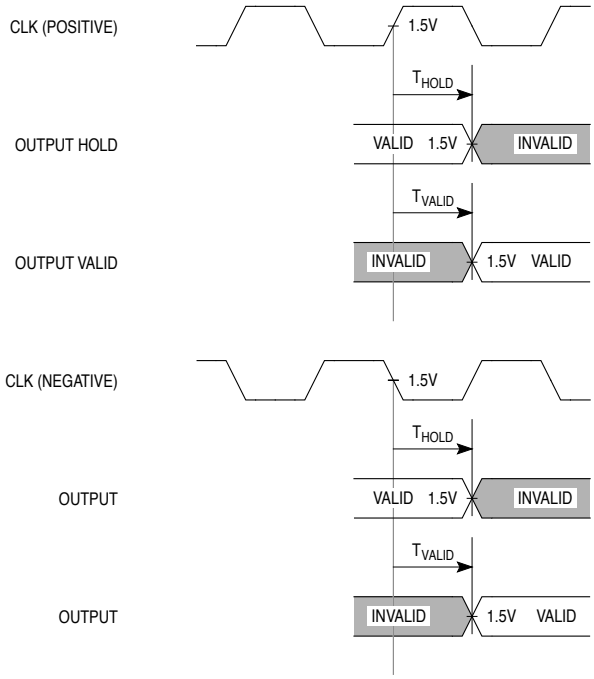
Input Timing Waveform Requirements

16.3.5 Processor Bus Output Timing Specifications

NAME	CHARACTERISTIC*	16.67 MHz		25 MHz		33.33 MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
CONTROL OUTPUTS								
B7a	CLK to $\overline{TS}$ Valid (signal from driven or three-state)	3	36	3	24	3	18	ns
B7b	CLK to $\overline{TA}$ Valid (signal from driven or three-state)	3	36	3	24	3	18	ns
B7c	CLK (falling) to $\overline{RAS}$[1:0] Valid	3	30	3	20	3	17	ns
B7d	CLK (falling) to $\overline{CAS}$[3:0] Valid	3	30	3	21	3	18	ns
B7e	CLK to $\overline{DRAMW}$ Valid	3	36	3	24	3	18	ns
B7f	CLK to $\overline{BR}$, $\overline{BD}$ Valid	3	36	3	24	3	18	ns
B7g	CLK to $\overline{RSTO}$ Valid	3	36	3	24	3	20	ns
B7h	CLK to PST[3:0], DDATA[3:0], DSO Valid	3	36	3	24	3	21	ns
B8a	CLK to Control Output ($\overline{TS}$, $\overline{TA}$, $\overline{BR}$, $\overline{BD}$, $\overline{RAS}$[1:0], $\overline{DRAMW}$, PST[3:0], DDATA[3:0], DSO, $\overline{RSTO}$) Invalid (Output Hold)	3	–	3	–	3	–	ns
B8b	CLK (rising or falling) to $\overline{CAS}$[3:0] Invalid (Output Hold)	3	–	3	–	3	–	ns
B9	CLK to Control Output ($\overline{TS}$, $\overline{TA}$) High Impedance	–	48	–	32	–	24	ns
ADDRESS AND ATTRIBUTE OUTPUTS								
B10	CLK to Address or Attribute Output (A[27:0], TT[1:0], ATM, SIZ[1:0], R/$\overline{W}$, $\overline{CS}$[7:0], $\overline{WE}$[3:0]) Valid (signal from driven or three-state)	3	36	3	26	3	22	ns
B11	CLK to Address or Attribute Output (A[27:0], TT[1:0], ATM, SIZ[1:0], R/$\overline{W}$, $\overline{CS}$[7:0], $\overline{WE}$[3:0]) Invalid (Output Hold)	3	–	3	–	3	–	ns
B12	CLK to Address or Attribute Output (A[27:0], TT[1:0], ATM, SIZ[1:0], R/$\overline{W}$, $\overline{CS}$[7:0], $\overline{WE}$[3:0]) High Impedance	–	48	–	32	–	24	ns
DATA OUTPUTS								
B13	CLK to Data Output (D[31:0]) Valid (signal from driven or three-state)	3	36	3	25	3	20	ns
B14	CLK to Data Output (D[31:0]) Invalid (Output Hold)	3	–	3	–	3	–	ns
B15	CLK to Data Output (D[31:0]) High Impedance	–	48	–	32	–	24	ns
OTHER OUTPUTS								
B16	$\overline{HIZ}$ to output tristated ($\overline{HIZ}$ asserted)	3	60	3	40	3	30	ns
B17	$\overline{HIZ}$ to output driven valid ($\overline{HIZ}$ negated)	3	60	3	40	3	30	ns

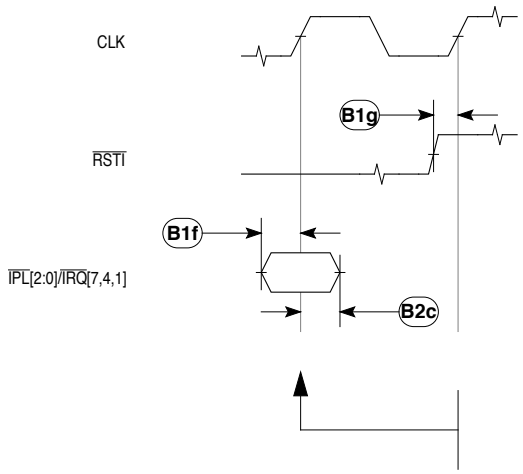
* Output timing is measured at the pin. Output specifications assume a capacitive load of 50pF.

16.3.6 Output Timing Waveform Diagram

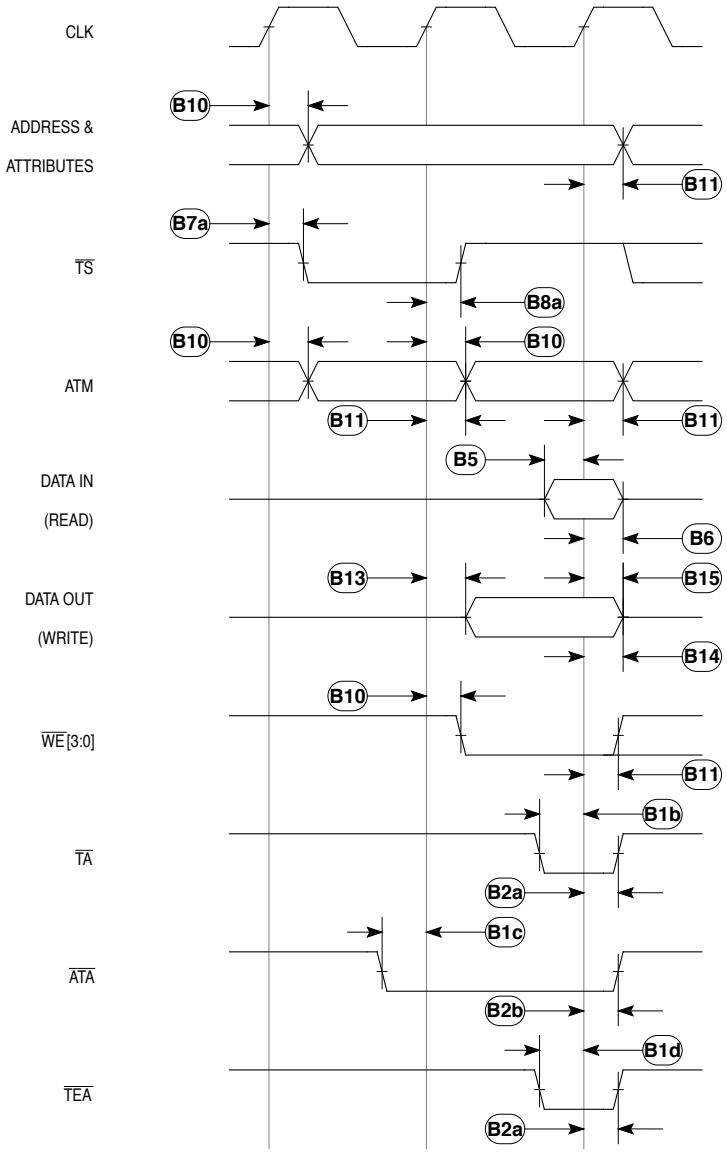


Output Timing Waveform

16.3.7 Processor Bus Timing Diagrams

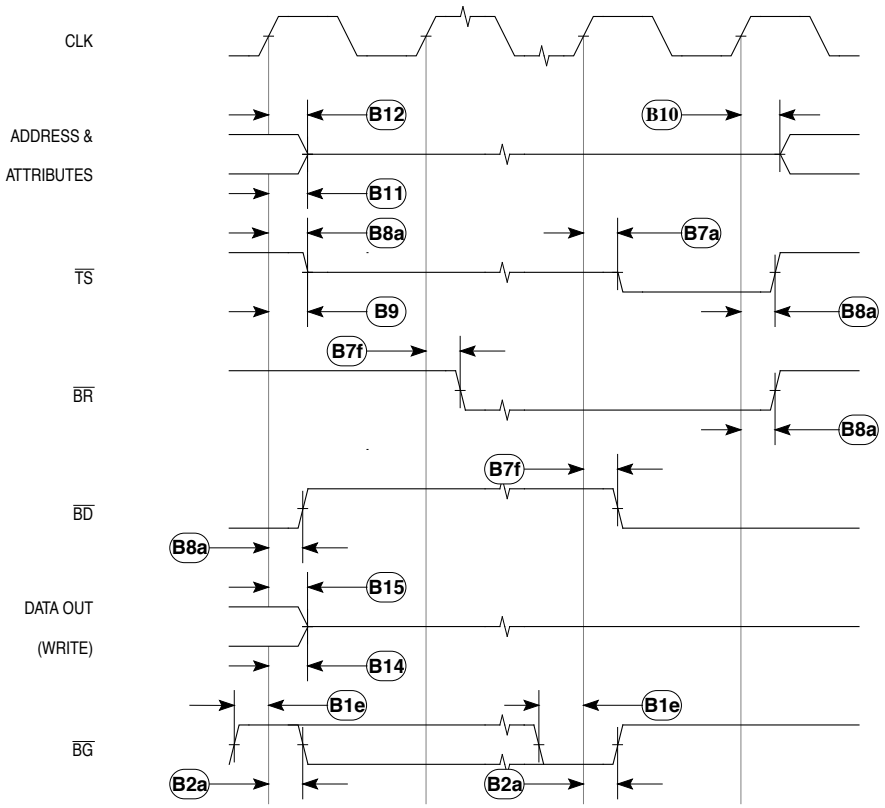


Reset Configuration Timing



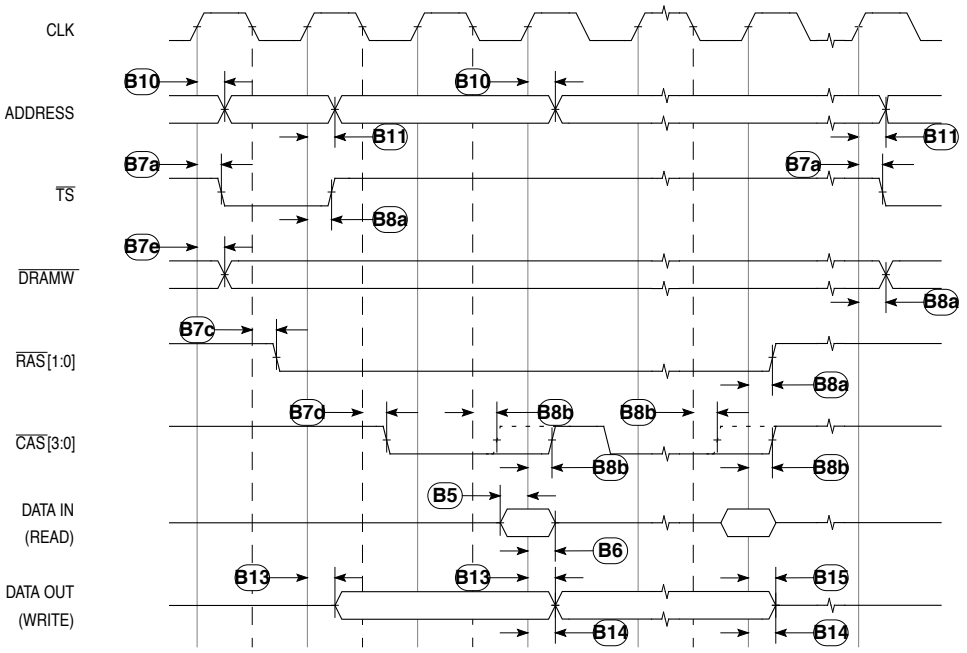
NOTE: ADDRESS AND ATTRIBUTES REFER TO THE FOLLOWING SIGNALS:
A[27:0], SIZ[1:0], R/W, TT[1:0], ATM, AND CS[7:0].

Read and Write Timing

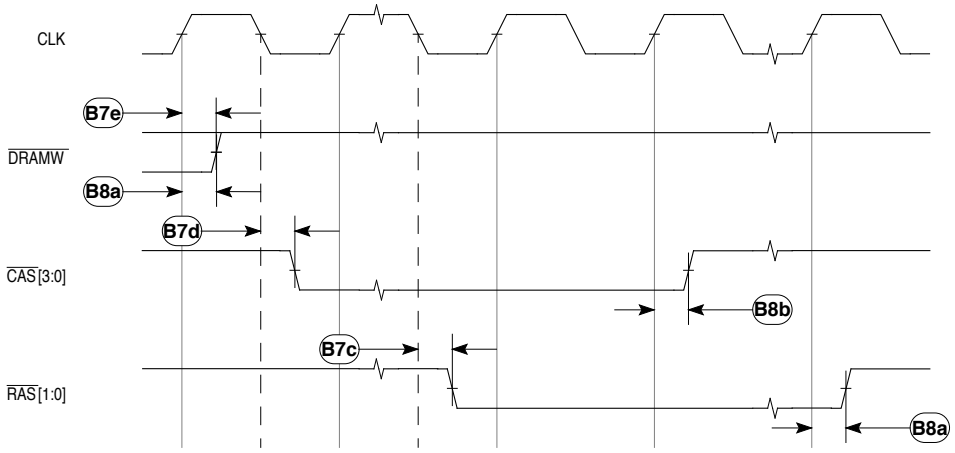


NOTE: ADDRESS AND ATTRIBUTES REFER TO THE FOLLOWING SIGNALS:
A[27:0], SIZ[1:0], R/W, TT[1:0], ATM, CS[7:0] AND WE[3:0].

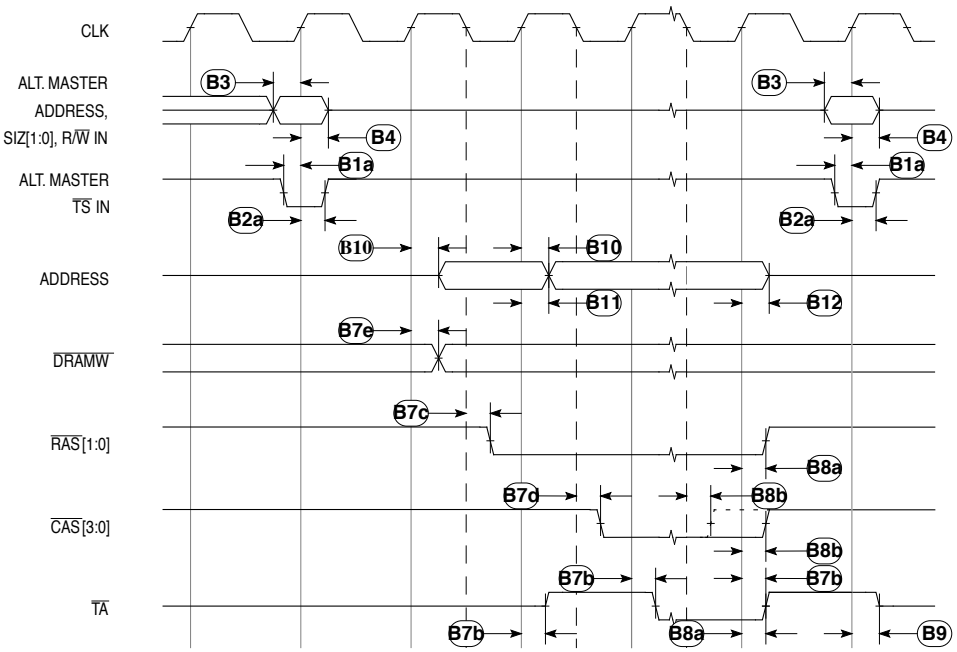
Bus Arbitration Timing



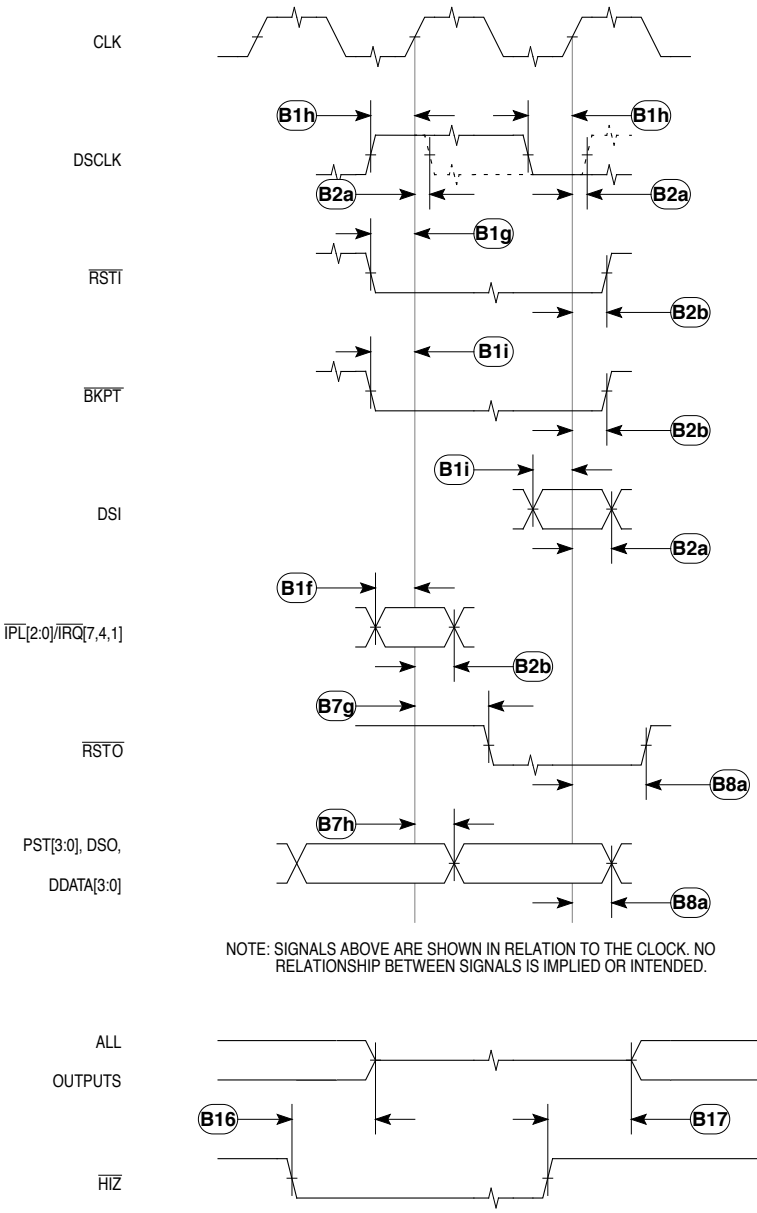
DRAM Signal Timing



DRAM Refresh Cycle Timing



DRAM Control By Alternate Master Timing

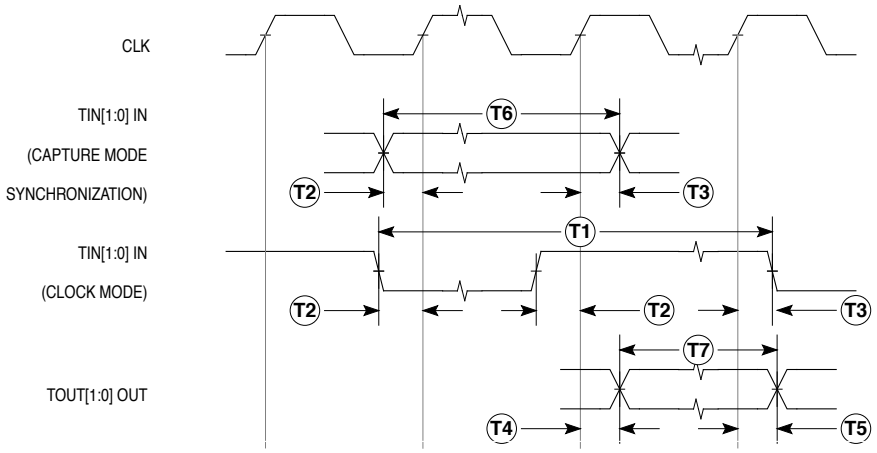


Miscellaneous Signal Timing

16.3.8 Timer Module AC Timing Specifications

NAME	CHARACTERISTIC	16.67 MHz		25 MHz		33.33 MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
T1	TIN[1:0] cycle time	3	—	3	—	3	—	clk
T2	TIN[1:0] Valid to CLK (Setup)	15	—	10	—	7	—	ns
T3	CLK to TIN[1:0] Invalid (Hold)	3	—	3	—	3	—	ns
T4	CLK to TOUT[1:0] Valid	3	36	3	24	3	18	ns
T5	CLK to TOUT[1:0] Invalid (Output Hold)	3	—	3	—	3	—	ns
T6	TIN[1:0] pulse width	1	—	1	—	1	—	clk
T7	TOUT[1:0] pulse width	1	—	1	—	1	—	clk

16.3.9 Timer Module Timing Diagram

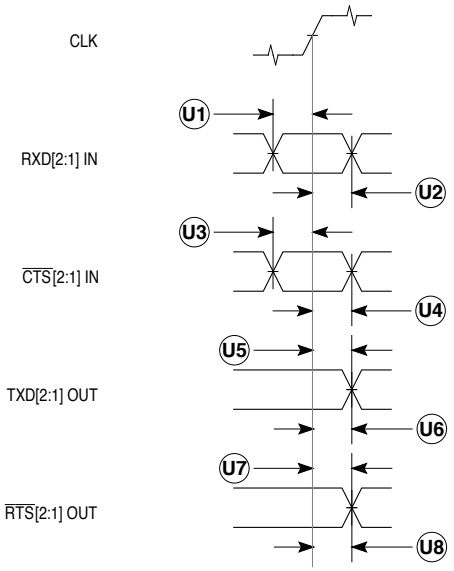


Timer Timing

16.3.10 UART Module AC Timing Specifications

NAME	CHARACTERISTIC	16.67 MHz		25 MHz		33.33 MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
U1	RxD[2:1] Valid to CLK (Setup)	15	—	10	—	7	—	ns
U2	CLK to RxD[2:1] Invalid (Hold)	3	—	3	—	2	—	ns
U3	$\overline{\text{CTS}}$[2:1] Valid to CLK (Setup)	15	—	10	—	7	—	ns
U4	CLK to $\overline{\text{CTS}}$[2:1] Invalid (Hold)	3	—	3	—	3	—	ns
U5	CLK to TxD[2:1] Valid	3	36	3	24	3	18	ns
U6	CLK to TxD[2:1] Invalid (Output Hold)	3	—	3	—	3	—	ns
U7	CLK to $\overline{\text{RTS}}$[2:1] Valid	3	36	3	24	3	20	ns
U8	CLK to $\overline{\text{RTS}}$[2:1] Invalid (Output Hold)	3	—	3	—	3	—	ns

16.3.11 UART Module Timing Diagram



UART Timing

16.3.12 M-BUS Module AC Timing Specifications

16.3.12.1 INPUT TIMING SPECIFICATIONS BETWEEN SCL AND SDA.

NAME	CHARACTERISTIC	16.67 MHz		25 MHz		33.33 MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
M1[1]	Start condition hold time	2	–	2	–	2	–	CLKs
M2[1]	Clock low period	8	–	8	–	8	–	CLKs
M3	SCL/SDA rise time (from V_l=0.5V to V_h=2.4V)	–	1	–	1	–	1	ms
M4	Data hold time	0	–	0	–	0	–	ns
M5	SCL/SDA fall time (from V_h=2.4V to V_l=0.5V)	–	1	–	1	–	1	ms
M6[1]	Clock high time	4	–	4	–	4	–	CLKs
M7	Data setup time	0	–	0	–	0	–	ns
M8[1]	Start condition setup time (for repeated start condition only)	2	–	2	–	2	–	CLKs
M9[1]	Stop condition setup time	2	–	2	–	2	–	CLKs

[1] Note: Units for these specifications are in processor CLK units.

16.3.12.2 OUTPUT TIMING SPECIFICATIONS BETWEEN SCL AND SDA.

NAME	CHARACTERISTIC	16.67 MHz		25 MHz		33.33 MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
M1[1,2]	Start condition hold time	6	–	6	–	6	–	CLKs
M2[1,2]	Clock low period	10	–	10	–	10	–	CLKs
M3[3]	SCL/SDA rise time (from V_l=0.5V to V_h=2.4V)	–	–	–	–	–	–	ms
M4[1,2]	Data hold time	7	–	7	–	7	–	CLKs
M5[4]	SCL/SDA fall time (from V_h=2.4V to V_l=0.5V)	–	TBD	–	TBD	–	TBD	ns
M6[1,2]	Clock high time	10	–	10	–	10	–	CLKs
M7[1,2]	Data setup time	2	–	2	–	2	–	CLKs
M8[1,2]	Start condition setup time (for repeated start condition only)	20	–	20	–	20	–	CLKs
M9[1,2]	Stop condition setup time	10	–	10	–	10	–	CLKs

[1] Note: Units for these specifications are in processor CLK units.
[2] Note: Output numbers are dependent on the value programmed into the MFDR; an MFDR programmed with the maximum frequency (MFDR = 0x20) will result in minimum output timings as shown in the above table. The MBUS interface is designed to

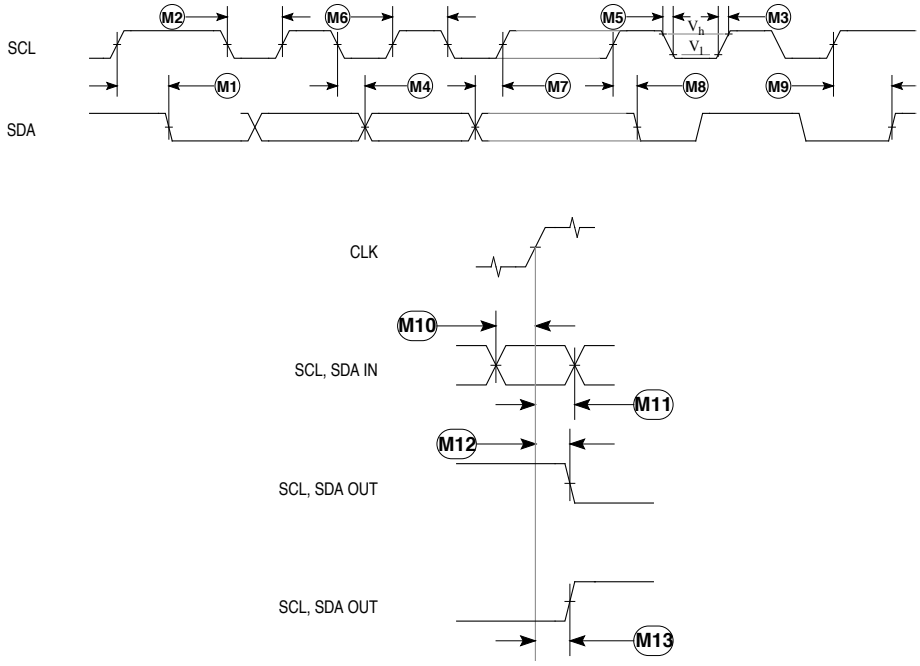
scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the MFDR; however, numbers given in the above table are the minimum values.
[3] Since SCL and SDA are open-collector -type outputs, which the processor can only actively drive low, the time required for SCL or SDA to reach a high level depends on external signal capacitance and pull-up resistor values.
[4] Specified at a nominal 50pF load.

16.3.12.3 TIMING SPECIFICATIONS BETWEEN CLK AND SCL, SDA.

NAME	CHARACTERISTIC	16.67 MHz		25 MHz		33.33 MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
M10	SCL, SDA Valid to CLK (Setup)	15	—	10	—	7	—	ns
M11	CLK to SCL, SDA Invalid (Hold)	3	—	3	—	3	—	ns
M12[1]	CLK to SCL, SDA Valid Low	3	36	3	24	3	18	ns
M13[2]	CLK to SCL, SDA Invalid (Output Hold)	3	—	3	—	3	—	ns

[1] Since SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, this specification applies only when SCL or SDA are driven low by the processor. The time required for SCL or SDA to reach a high level depends on external signal capacitance and pull-up resistor values.
[2] Since SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, this specification applies only when SCL or SDA are actively being driven or held low by the processor.

16.3.13 M-Bus Module Timing Diagram

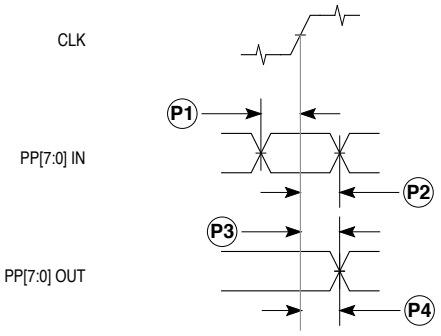


M-Bus Timing

16.3.14 General-Purpose I/O Port AC Timing Specifications

NAME	CHARACTERISTIC	16.67 MHz		25 MHz		33.33 MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
P1	PP[7:0]input setup time to CLK (rising)	15	–	10	–	7	–	ns
P2	PP[7:0] input hold time from CLK (rising)	3	–	3	–	3	–	ns
P3	CLK to PP[7:0] Output Valid	3	36	3	24	3	21	ns
P4	CLK to PP[7:0] Output Invalid (Output Hold)	3	–	3	–	3	–	ns

16.3.15 General-Purpose I/O Port Timing Diagram

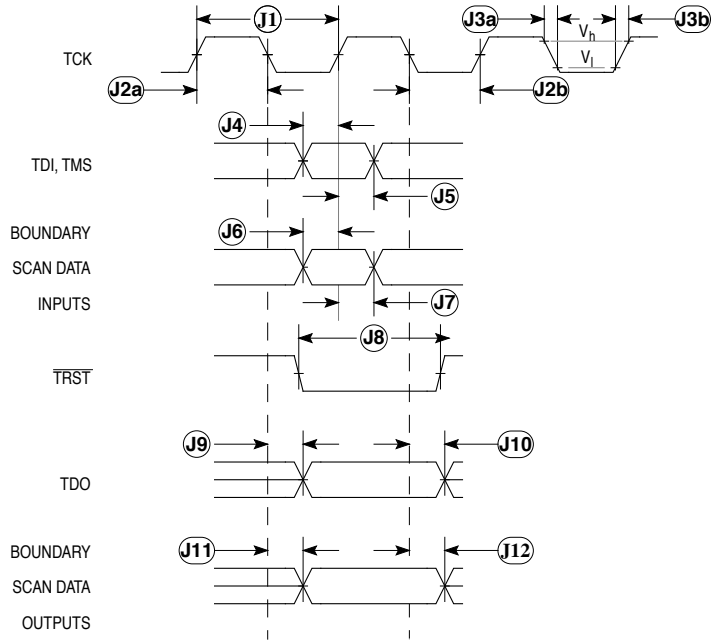


General-Purpose I/O Port Timing

16.3.16 IEEE 1149.1 (JTAG) AC Timing Specifications

NAME	CHARACTERISTIC	16.67 MHz		25 MHz		33.33 MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
—	TCK frequency of operation	0	10	0	10	0	10	MHz
J1	TCK cycle time	100	—	100	—	100	—	ns
J2a	TCK clock pulse high width measured at 1.5V	40	—	40	—	40	—	ns
J2b	TCK clock pulse low width measured at 1.5V	40	—	40	—	40	—	ns
J3a	TCK fall time (from V_h=2.4V to V_l=0.5V)	—	5	—	5	—	5	ns
J3b	TCK rise time (from V_l=0.5V to V_h=2.4V)	—	5	—	5	—	5	ns
J4	TDI, TMS to TCK rising (Setup)	10	—	10	—	10	—	ns
J5	TCK rising edge to TDI, TMS Invalid (Hold)	15	—	15	—	15	—	ns
J6	Boundary scan data valid to TCK rising edge (Setup)	10	—	10	—	10	—	ns
J7	Boundary scan data invalid to TCK rising edge (Hold)	15	—	15	—	15	—	ns
J8	$\overline{TRST}$ pulse width (asynchronous to clock edges)	15	—	15	—	15	—	ns
J9	TCK falling edge to TDO valid (signal from driven or three-state)	—	30	—	30	—	30	ns
J10	TCK falling edge to TDO high impedance	—	30	—	30	—	30	ns
J11	TCK falling edge to boundary scan data valid (signal from driven or three-state)	—	35	—	35	—	35	ns
J12	TCK falling edge to boundary scan data high impedance	—	30	—	30	—	30	ns

16.3.17 IEEE 1149.1 (JTAG) Timing Diagram



IEEE 1149.1 (JTAG) Timing