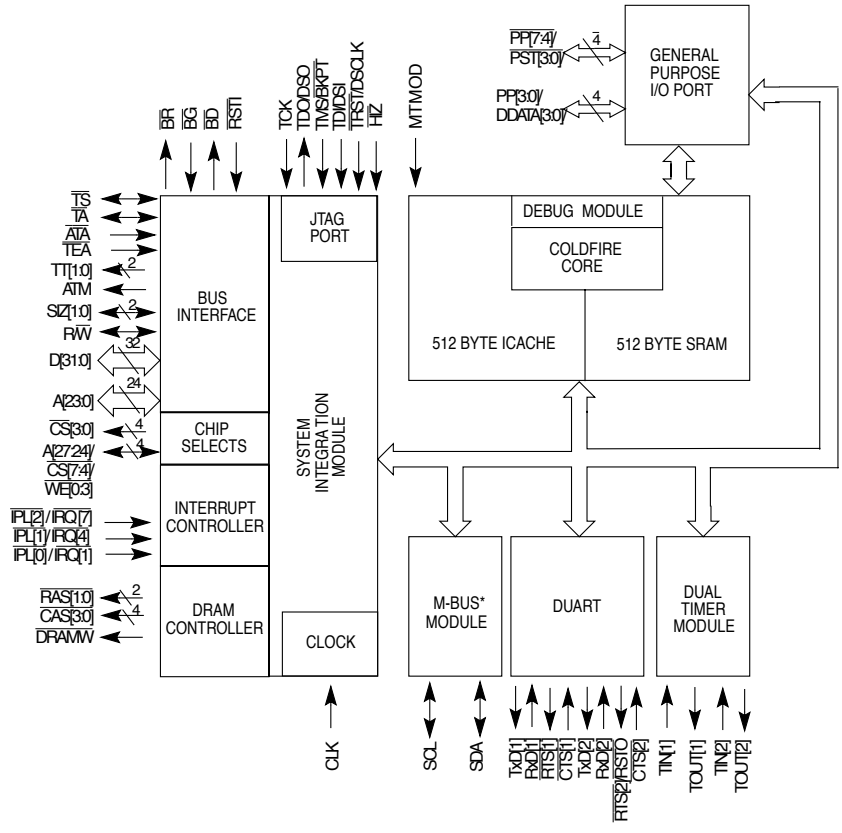
SECTION 2
SIGNAL DESCRIPTION

2.1 INTRODUCTION

Figure 2-1 displays the block diagram of the MCF5206 along with the signal interface. This section describes the MCF5206 input and output signals. The descriptions are grouped according to functionality (refer to Table 2-1).



*M-Bus is compatible with Philips' I²C interface

Figure 2-1. MCF5206 Block Diagram

NOTE

The terms assert and negate are used throughout this section to avoid confusion when dealing with a mixture of active-low and active-high signals. The term assert or assertion indicates that a signal is active or true, independent of the level represented by a high or low voltage. The term negate or negation indicates that a signal is inactive or false.

Table 2-1. MCF5206 Signal Index

SIGNAL NAME	MNEMONIC	FUNCTION	INPUT/ OUTPUT
Address[27:24]/ Chip-Select[7:4]/ Write Enable[0:3]	A[27:24]/ $\overline{CS}$[7:4]/ $\overline{WE}$[0:3]	Upper four bits of the address bus/ Upper four chip-selects enable peripherals at programmed addresses/ Write enables select individual bytes in memory	In,Out/ Out/ Out
Address	A[23:0]	Lower 24 bits of the address bus. A[4:2] indicate the interrupt level during an IACK cycle	In,Out
Data	D[31:0]	Data bus used to transfer byte, word, or longword data	In,Out
Chip-Select[3:0]	$\overline{CS}$[3:0]	Enables peripherals at programmed addresses. $\overline{CS}$[1] can indicate IACK during an interrupt acknowledge cycle. $\overline{CS}$[0] provides relocatable boot ROM capability	Out
Interrupt Priority Level/ Interrupt Request	$\overline{IPL}$[2]/$\overline{IRQ}$[7] $\overline{IPL}$[1]/$\overline{IRQ}$[4] $\overline{IPL}$[0]/$\overline{IRQ}$[1]	Provides encoded interrupt priority level to processor/ Three individual external interrupts set to levels 7, 4, 1	In/ In
Read/Write	R/$\overline{W}$	Identifies read and write data transfers	In,Out
Size	SIZ[1:0]	Indicates the data transfer size	In,Out
Transfer Type	TT[1:0]	Indicates the transfer type: normal, CPU space/Interrupt acknowledge or emulator mode	Out
Access Type & Mode	ATM	Time-multiplexed output signal indicating access type (instruction or data) and access mode (supervisor or user)	Out
Transfer Start	$\overline{TS}$	Indicates the beginning of a bus cycle	In,Out
Transfer Acknowledge	$\overline{TA}$	Synchronous transfer acknowledge. Asserted to indicate the successful completion of a bus transfer.	In,Out
Asynchronous Transfer Acknowledge	$\overline{ATA}$	Asynchronous transfer acknowledge. Asserted to indicate the successful completion of a bus transfer	In
Transfer Error Acknowledge	$\overline{TEA}$	Asserted to indicate an error condition exists for a bus transfer	In
Bus Request	$\overline{BR}$	Asserted by the MCF5206 to request bus mastership	Out
Bus Grant	$\overline{BG}$	Asserted by bus arbiter to grant bus mastership privileges to the MCF5206	In
Bus Driven	$\overline{BD}$	Indicates the MCF5206 has assumed explicit bus mastership of the external bus	Out
Clock Input	CLK	Input used to clock internal logic	In
Reset	$\overline{RSTI}$	Processor reset	In
Row Address Strobe	$\overline{RAS}$[1:0]	Row address strobe for external DRAM	Out
Column Address Strobe	$\overline{CAS}$[3:0]	Column address strobe for external DRAM	Out
DRAM Write	$\overline{DRAMW}$	Asserted on DRAM write cycles and negated on DRAM read cycles	Out
Receive Data	RxD[1], RxD[2]	Receive serial data input for UART1 and UART2	In
Transmit Data	TxD[1],TxD[2]	Transmit serial data output for UART1 and UART2	Out
Request-To-Send	$\overline{RTS}$[1]	Indicates UART1 is ready to receive data	Out
Request-To-Send/ Reset Out	$\overline{RTS}$[2]/$\overline{RSTO}$	$\overline{RTS}$[2] indicates UART2 is ready to receive data/ $\overline{RTSO}$ is the reset out signal	Out/ Out
Clear-To-Send	$\overline{CTS}$[1], $\overline{CTS}$[2]	Indicates can transmit serial data for UART1 and UART2	In

Table 2-1. MCF5206 Signal Index (Continued)

SIGNAL NAME	MNEMONIC	FUNCTION	INPUT/ OUTPUT
Timer Input	TIN[1], TIN[2]	Clock input to timer or trigger input for timer value capture logic	In
Timer Output	TOUT[1], TOUT[2]	Timer output waveform or pulse generation	Out
Serial Clock Line	SCL	Clock signal for M-Bus module operation	In,Out
Serial Data Line	SDA	Serial data port for M-Bus module operation	In,Out
General Purpose I/O/ Processor Status	PP[7:4]/PST[3:0]	Upper 4 bits of general purpose I/O port / Internal processor status.	In.Out/ Out
General Purpose I/O/ Debug Data	PP[3:0]/DDATA[3:0]	Lower 4 bits of general purpose I/O port / Captured processor data and break-point status debug data	In,Out/ Out
Test Clock	TCK	JTAG clock signal	In
Test Data Output/ Development Serial Output	TDO/DSO	JTAG serial data out/ Debug serial out	Out/ Out
Test Mode Select/ Break Point	TMS/$\overline{\text{BKPT}}$	JTAG mode select/ Debug mode breakpoint	In/ In
Test Data Input / Development Serial Input	TDI/DSI	JTAG serial data input/ Debug serial input	In/ In
Test Reset/ Development Serial Clock	$\overline{\text{TRST}}$/DSCLK	Asynchronous JTAG reset input/ Debug serial clock input	In/ In
Motorola Test Mode	MTMOD	Selects JTAG or Debug signals	In
High Impedance	$\overline{\text{HIZ}}$	Output buffer three-state and master reset control	In

2.2 ADDRESS BUS

These three-state bidirectional address signals indicate the following:

Table 2-2. Address Bus

TYPE OF BUS TRANSFER/MEMORY SPACE ACCESSED	ADDRESS BUS
Interrupt Acknowledge Transfer	A[27:5] = $7FFFF, A[1:0]=$0, A[4:2] Interrupt Level being serviced
Chip-Select Transfer	Address of byte or most significant byte of word or longword being accessed
DRAM Transfer	Row Address and Column Address indicating byte or most significant byte of word or longword being accessed
Default Memory	Address of byte or most significant byte of word or longword being accessed

The address bus includes 24 dedicated address signals, A[23:0], and supports as many as four additional configurable address signals, A[27: 24] (refer to **Section 7.3.2.10 Pin Assignment Register (PAR)**). The address will appear only on the pins configured to be address signals.

When an external master is using the MCF5206 as a slave DRAM controller, the external master asserts $\overline{\text{TS}}$ and places the transfer address on the address pins. The external master then three-states the address signals and the MCF5206 drives the row address and the column address on the address bus at the appropriate times.

2.2.1 Address Bus (A[27:24]/ $\overline{\text{CS}}$[7:4]/ $\overline{\text{WE}}$[0:3])

These multiplexed pins can serve as the most significant nibble of the address pins, chip-selects, or as write enables. Programming the Pin Assignment Register (PAR) in the SIM determines the function of each of these four multiplexed pins. During reset, these pins are configured to be write enables.

When any of these pins are enabled as address lines in the PAR, they represent the most significant bits of the address bus. A maximum of 256 Mbytes of memory is addressable when all of these pins are programmed as address signals. Any of these pins that are programmed as address lines have the same timing as the lower address lines A[23:0]. All address lines become valid during the same time $\overline{\text{TS}}$ is asserted.

2.2.2 Address Bus (A[23:0])

The three-state bidirectional signals are the 24 least significant bits of the address bus. For chip-select and default memory transfers initiated by the ColdFire core, the MCF5206 outputs the address and increments the lower bits during burst transfers, allowing the address bus to be directly connected to external memory. For DRAM transfers initiated by the ColdFire core, the MCF5206 outputs the row address and column address as specified by the DRAM control registers.

The MCF5206 does not output the address during alternate master initiated chip-select and default memory transfers. When an external master is using the MCF5206 as a slave DRAM controller, the external master asserts $\overline{\text{TS}}$ and places the row and column address on the address pins. The external master drives the address signals to a high-impedence state and the MCF5206 then drives the row address and the column address on the address bus at the appropriate times.

2.2.3 Data Bus (D[31:0])

The three-state bidirectional signals provide a nonmultiplexed general-purpose data path between the MCF5206 and all other devices in the system. During a read bus transfer, data is registered from the bus on the rising clock edge in which $\overline{\text{TA}}$ is asserted, or during the rising clock in which internal asynchronous transfer acknowledge is asserted or internal transfer acknowledge is asserted.

The data bus port width is initially configured by the values on $\overline{\text{IPL}}$[1]/$\overline{\text{IRQ4}}$ and $\overline{\text{IPL}}$[0]/ $\overline{\text{IRQ1}}$ during reset. Port width is individually programmed for each chip-select region and DRAM bank, and is globally configured for a memory region not matching chip-select settings or DRAM memory, referred to as default memory. The data bus transfers byte, word, or longword-sized data. All 32 bits of the data bus are driven during writes, regardless of port width or operand size.

2.3 CHIP-SELECTS

The MCF5206 provides as many eight programmable chip-selects that can directly interface with SRAM, EPROM, EEPROM, and peripherals.

2.3.1 Chip-Selects (A[27:24]/ $\overline{\text{CS[7:4]}}$/ $\overline{\text{WE[0:3]}}$)

These multiplexed pins can serve as the most significant nibble of the address pins, chip-selects, or as write enables. Programming the Pin Assignment Register (PAR) in the SIM determines the function of each of these four multiplexed pins. During reset, these pins are configured to be write-enables.

The active-low chip-select output signals provide control for peripherals and memory. You can program each chip-select for an address location, with masking capabilities, port size and burst-capability indication, wait-state generation, and internal/external termination. A reset disables these chip-selects.

2.3.2 Chip-Selects ($\overline{\text{CS[3:0]}}$)

These active-low output signals provide control for peripherals and memory. $\overline{\text{CS[3]}}$ and $\overline{\text{CS[2]}}$ are functionally equivalent to the upper order chip-selects previously described. However, $\overline{\text{CS[1]}}$ can also be programmed to assert during CPU space accesses including interrupt-acknowledge cycles. $\overline{\text{CS[0]}}$ provides a special function as a global chip-select that lets you relocate boot ROM at any defined address space. $\overline{\text{CS[0]}}$ is the only chip-select initialized during reset. Port size and termination (internal vs. external) for $\overline{\text{CS[0]}}$ are configured by the logic levels on $\overline{\text{IPL[2]}}$/$\overline{\text{IRQ[7]}}$, $\overline{\text{IPL[1]}}$/$\overline{\text{IRQ[4]}}$, and $\overline{\text{IPL[0]}}$/$\overline{\text{IRQ[1]}}$ during reset.

2.3.3 Byte Write-Enables (A[27:24]/ $\overline{\text{CS[7:4]}}$/ $\overline{\text{WE[0:3]}}$)

These multiplexed pins can serve as the most significant nibble of the address pins, chip-selects, or as write-enables. Programming the Pin Assignment Register (PAR) in the SIM determines the function of each of these four multiplexed pins. During reset, these pins are configured to be write-enables.

The active-low write-enable output signals provide control for peripherals and memory during write transfers. During write transfers, these outputs indicate which bytes within a longword transfer are being selected and which bytes of the data bus will be used for the transfer. $\overline{\text{WE[0]}}$ controls D[31:24], $\overline{\text{WE[1]}}$ controls D[23:16], $\overline{\text{WE[2]}}$ controls D[15:8] and $\overline{\text{WE[3]}}$ controls D[7:0]. These generated signals provide byte data select signals that are decoded from the SIZ[1:0] and A[1:0] signals in addition to the programmed port size and burst capability of the memory being accessed, as shown in Table 2-3.

2.4 INTERRUPT CONTROL SIGNALS

The interrupt signals supply the external interrupt requests or interrupt level to the MCF5206. During reset, these pins configure the processor for the number of wait states and port size for the boot chip-select ($\overline{\text{CS[0]}}$).

Table 2-3. Byte Write-Enable Signals

TRANSFER SIZE	PORT SIZE	BURST	SIZ1	SIZ0	A1	A0	$\overline{WE0}$	$\overline{WE1}$	$\overline{WE2}$	$\overline{WE3}$
							D31-D24	D23-D16	D15-D8	D7-D0
BYTE	8- bit	0	0	1	0	0	0	1	1	1
					0	1	0	1	1	1
					1	0	0	1	1	1
					1	1	0	1	1	1
		1	0	1	0	0	0	1	1	1
					0	1	0	1	1	1
					1	0	0	1	1	1
					1	1	0	1	1	1
	16- bit	0	0	1	0	0	0	1	1	1
					0	1	1	0	1	1
					1	0	0	1	1	1
					1	1	1	0	1	1
		1	0	1	0	0	0	1	1	1
					0	1	1	0	1	1
					1	0	0	1	1	1
					1	1	1	0	1	1
	32- bit	0	0	1	0	0	0	1	1	1
					0	1	1	0	1	1
					1	0	1	1	0	1
					1	1	1	1	1	0
		1	0	1	0	0	0	1	1	1
					0	1	1	0	1	1
					1	0	1	1	0	1
					1	1	1	1	1	0
WORD	8- bit	0	0	1	0	0	0	1	1	1
					0	1	0	1	1	1
					1	0	0	1	1	1
					1	1	0	1	1	1
		1	1	0	0	0	0	1	1	1
					0	1	0	1	1	1
					1	0	0	1	1	1
					1	1	0	1	1	1
	16- bit	0	1	0	0	0	0	0	1	1
					1	0	0	0	1	1
		1	1	0	0	0	0	0	1	1
					1	0	0	0	1	1
	32 bit	0	1	0	0	0	0	0	1	1
					1	0	1	1	0	0
		1	1	0	0	0	0	0	1	1
					1	0	1	1	0	0

Table 2-3. Byte Write-Enable Signals (Continued)

TRANSFER SIZE	PORT SIZE	BURST	SIZ1	SIZ0	A1	A0	$\overline{WE0}$	$\overline{WE1}$	$\overline{WE2}$	$\overline{WE3}$
							D31-D24	D23-D16	D15-D8	D7-D0
LONGWORD	8-bit	0	0	1	0	0	0	1	1	1
					0	1	0	1	1	1
					1	0	0	1	1	1
					1	1	0	1	1	1
		1	0	0	0	0	0	1	1	1
					0	1	0	1	1	1
					1	0	0	1	1	1
					1	1	0	1	1	1
	16-bit	0	1	0	0	0	0	0	1	1
					1	0	0	0	1	1
		1	0	0	0	0	0	0	1	1
					1	0	0	0	1	1
	32-bit	0	0	0	0	0	0	0	0	0
		1	0	0	0	0	0	0	0	0
LINE	8-bit	0	0	1	0	0	0	1	1	1
					0	1	0	1	1	1
					1	0	0	1	1	1
					1	1	0	1	1	1
		1	1	1	0	0	0	1	1	1
					0	1	0	1	1	1
					1	0	0	1	1	1
					1	1	0	1	1	1
	16-bit	0	1	0	0	0	0	0	1	1
					1	0	0	0	1	1
		1	1	1	0	0	0	0	1	1
					1	0	0	0	1	1
	32-Bit	0	0	0	0	0	0	0	0	0
		1	1	1	0	0	0	0	0	0

2.4.1 Interrupt Priority Level/ Interrupt Request ($\overline{IPL[2]}$/$\overline{IRQ[7]}$,$\overline{IPL[1]}$/ $\overline{IRQ[4]}$, $\overline{IPL[0]}$/$\overline{IRQ[1]}$)

You can program these three active-low input pins as either interrupt priority-level signals ($\overline{IPL[2:0]}$) or predefined interrupt request pins ($\overline{IRQ[7]}$, $\overline{IRQ[4]}$, $\overline{IRQ[1]}$). Programming the Pin Assignment Register (PAR) in the SIM determines the function of these pins. During reset, these pins are configured to be predefined interrupt requests.

When these pins are programmed to be interrupt priority-level signals, $\overline{IPL[2:0]}$ signals the priority level (7-1) of an external interrupt; $\overline{IPL[2:0]}$=000 (level 7) indicates the highest unmaskable interrupt, while $\overline{IPL[2:0]}$=111 (level 0) indicates no interrupt request. When these pins are programmed to be interrupt-request signals, the assertion of $\overline{IRQ[7]}$ generates a level 7 interrupt, $\overline{IRQ[4]}$ generates a level 4 interrupt, and $\overline{IRQ[1]}$ generates a level 1 interrupt.

During reset, the interrupt-priority level/interrupt-request pins are sampled to define port size and wait-state generation for $\overline{CS}[0]$. Table 2-4 and Table 2-5 show the reset values for wait states and port size for $\overline{CS}[0]$ based on the these pins.

Table 2-4. Boot CS[0] Automatic Acknowledge (AA) Enable

$\overline{IPL[2]}$/ $\overline{IRQ[7]}$	INITIAL $\overline{CS[0]}$ AA
0	Disabled
1	Enabled with 15 wait states

Table 2-5. Interrupt Request Encodings for $\overline{CS[0]}$

$\overline{IPL[1]}$/ $\overline{IRQ[4]}$	$\overline{IPL[0]}$/ $\overline{IRQ[1]}$	INITIAL $\overline{CS[0]}$ PORT SIZE
0	0	32-bit port
0	1	8-bit port
1	0	16-bit port
1	1	16-bit port

2.5 BUS CONTROL SIGNALS

2.5.1 Read/Write (R/$\overline{W}$)

This three-state bidirectional signal defines the data transfer direction for the current bus cycle. A high (logic one) level indicates a read cycle while a low (logic zero) level indicates a write cycle. When an alternate bus master is controlling the bus, the MCF5206 monitors this signal to determine if chip-select or DRAM control signals need to be asserted.

2.5.2 Size (SIZ[1:0])

These three-state bidirectional signals indicate the transfer data size for the bus cycle. When an alternate bus master is controlling the bus, the MCF5206 monitors these signals to determine the data size for asserting the appropriate memory control signals. Table 2-6 shows the definitions of the SIZ[1:0] encoding.

Table 2-6. Data Transfer Size Encoding

SIZ[1:0]	DATA TRANSFER SIZE
00	Longword
01	Byte
10	Word
11	Line

2.5.3 Transfer Type (TT[1:0])

These three-state output signals indicate the type of access for the current bus cycle. TT[1:0] are not sampled by the MCF5206 during alternate master transfers. Table 2-7 lists the definitions of the TT[1:0] encodings.

Table 2-7. Bus Cycle Transfer Type Encoding

TT[1:0]	TRANSFER TYPE
0 0	Normal Access
0 1	Reserved
1 0	Emulator Access
1 1	CPU Space or Interrupt Acknowledge

2.5.4 Access Type and Mode (ATM)

This three-state output signal provides supplemental information for each transfer cycle type. ATM is not sampled by the MCF5206 during alternate master transfers. Table 2-8 lists the encoding for normal, debug and CPU space/interrupt-acknowledge transfer types.

Table 2-8. ATM Encoding

TRANSFER TYPE	INTERNAL TRANSFER MODIFIER	ATM (TS=0)	ATM (TS=1)
00 (Normal Access)	Supervisor Code	1	1
	Supervisor Data	0	1
	User Code	1	0
	User Data	0	0
10 (Debug Access)	Supervisor Code	1	1
	Supervisor Data	0	1
11 (CPU Space/ Acknowledge Access)	CPU Space - MOVEC Instruction	0	0
	Interrupt Acknowledge - level 7	1	0
	Interrupt Acknowledge - level 6	1	0
	Interrupt Acknowledge - level 5	1	0
	Interrupt Acknowledge - level 4	1	0
	Interrupt Acknowledge - level 3	1	0
	Interrupt Acknowledge - level 2	1	0
	Interrupt Acknowledge - level 1	1	0

2.5.5 Transfer Start ($\overline{TS}$)

The MCF5206 asserts this three-state bidirectional active-low signal for one clock period to indicate the start of each bus cycle. During alternate master accesses, the MCF5206 monitors transfer start ($\overline{TS}$) to detect the start of each alternate master bus cycle to determine if chip-select or DRAM control signals need to be asserted.

2.5.6 Transfer Acknowledge ($\overline{TA}$)

This three-state bidirectional active-low synchronous signal indicates the completion of a requested data transfer operation. During transfers initiated by the MCF5206, transfer acknowledge ($\overline{TA}$) is an input signal from the referenced slave device indicating completion of the transfer.

$\overline{TA}$ is not used for termination during DRAM accesses initiated by the MCF5206.

When an alternate master is controlling the bus, $\overline{TA}$ may be driven as an output by the MCF5206 or may be driven by the referenced slave device to indicate the completion of the requested data transfer. If the alternate master requested transfer is to a chip-select or default memory, the assertion of $\overline{TA}$ is controlled by the number of wait states and the setting of the Alternate Master Automatic Acknowledge (EMAA) bit in the Chip-Select Control Registers (CSCRs) or the Default Memory Control Register (DMCR). If the alternate master requested transfer is a DRAM access, $\overline{TA}$ is driven by the MCF5206 as an output and asserted at the completion of the transfer.

2.5.7 Asynchronous Transfer Acknowledge ($\overline{ATA}$)

This active-low asynchronous input signal indicates the completion of a requested data transfer operation. Asynchronous transfer acknowledge ($\overline{ATA}$) is an input signal from the referenced slave device indicating completion of the transfer. $\overline{ATA}$ is synchronized internal to the MCF5206.

NOTE

The internal synchronized version of asynchronous transfer acknowledge ($\overline{ATA}$) will be referred to as “internal asynchronous transfer acknowledge ($\overline{ATA}$).” Because of the time required to internally synchronize $\overline{ATA}$ during a read cycle, data is latched on the rising edge of CLK when the internal $\overline{ATA}$ is asserted. Consequently, data must remain valid for at least one CLK cycle after the assertion of $\overline{ATA}$. Similarly, during a write cycle, data is driven until the rising edge of CLK when the internal $\overline{ATA}$ is asserted.

$\overline{ATA}$ must be driven for one full CLK to ensure that the MCF5206 properly synchronizes the signal. $\overline{ATA}$ is not used for termination during DRAM accesses.

2.5.8 Transfer Error Acknowledge ($\overline{TEA}$)

This active-low input signal is asserted by the external slave to indicate an error condition for the current transfer. The assertion of transfer error acknowledge ($\overline{TEA}$) will cause the MCF5206 to immediately abort the bus cycle. The assertion of $\overline{TEA}$ has precedence over the assertion of $\overline{ATA}$ and $\overline{TA}$.

NOTE

$\overline{TEA}$ can be asserted to a maximum of one clock after the assertion of $\overline{ATA}$ and still be recognized.

$\overline{TEA}$ has no effect during DRAM accesses.

2.6 BUS ARBITRATION SIGNALS

2.6.1 Bus Request ($\overline{BR}$)

This active-low output signal indicates to an external arbiter that the MCF5206 needs use of the bus for one or more bus cycles. $\overline{BR}$ is negated when the MCF5206 begins an access to the external bus, and remains negated until another internal request occurs with $\overline{BG}$ negated.

2.6.2 Bus Grant ($\overline{BG}$)

An external arbiter asserts this active-low input signal to indicate that the MCF5206 can become master of the external bus at the next rising edge of CLK. When the arbiter negates $\overline{BG}$, the MCF5206 relinquishes the bus as soon as the current transfer is complete, provided the bus lock bit in the SIMR is not set. If the bus lock bit is set, the MCF5206 will retain bus mastership until the bus lock bit is cleared. The external arbiter must not grant the bus to any other master until the MCF5206 negates $\overline{BD}$.

2.6.3 Bus Driven ($\overline{BD}$)

The MCF5206 asserts this active-low output signal to indicate it has assumed explicit mastership of the external bus. The MCF5206 will assert $\overline{BD}$ if $\overline{BG}$ is asserted and either the MCF5206 has a pending bus transfer or the bus lock bit in the SIMR is set to 1. If the MCF5206 is granted mastership of the external bus, but does not have a pending bus transfer and the bus lock bit in the SIMR is cleared, the $\overline{BD}$ signal is not asserted (implicit mastership of the bus is assumed).

If $\overline{BG}$ is negated to the MCF5206 during a bus transfer and the bus lock bit in the SIMR is cleared, the MCF5206 will complete the last transfer of the current access, negate $\overline{BD}$, and three-state all bus signals on the rising edge of CLK. If the MCF5206 loses bus ownership during an idle bus period with $\overline{BD}$ asserted and the bus lock bit in the SIMR cleared, the MCF5206 will negate $\overline{BD}$ and three-state all bus signals on the next rising edge of CLK. If the MCF5206 loses bus ownership during an idle bus period with $\overline{BD}$ asserted and the bus lock bit in the SIMR set to 1, the MCF5206 will continue to assert $\overline{BD}$ and will maintain explicit ownership of the external bus until the bus lock bit in the SIMR is cleared.

2.7 CLOCK AND RESET SIGNALS

2.7.1 Clock Input (CLK)

CLK is the MCF5206 synchronous clock, and clocks or sequences the MCF5206 internal logic and external signals.

2.7.2 Reset ($\overline{\text{RSTI}}$)

Asserting the active-low $\overline{\text{RSTI}}$ input will cause the MCF5206 processor to enter reset exception processing. When $\overline{\text{RSTI}}$ is recognized, the address bus, data bus, TT, SIZ, R/$\overline{\text{W}}$, ATM and $\overline{\text{TS}}$ will be three-stated; $\overline{\text{BR}}$ and $\overline{\text{BD}}$ will be negated.

If $\overline{\text{RSTI}}$ is asserted with $\overline{\text{HIZ}}$ asserted, the MCF5206 enters master reset mode. In this reset mode, the entire MCF5206 (including the DRAM controller refresh circuitry) is reset. You must use master reset for all power-on resets.

If $\overline{\text{RSTI}}$ is asserted with $\overline{\text{HIZ}}$ negated, the MCF5206 enters normal reset mode. In this reset mode, the DRAM controller refresh circuitry will not be reset and will continue to generate refresh cycles at the programmed rate and with the programmed waveform timing.

2.7.3 Reset Out ($\overline{\text{RTS[2]}}$/$\overline{\text{RSTO}}$)

$\overline{\text{RTS[2]}}$ is multiplexed with the $\overline{\text{RSTO}}$ signal. Programming the Pin Assignment Register (PAR) in the SIM determines the function of this pin. During reset, this pin is configured to be $\overline{\text{RSTO}}$.

$\overline{\text{RSTO}}$ is an output that drives peripherals to reset. There will be no more than two clocks from the assertion of $\overline{\text{RSTI}}$ to the assertion of $\overline{\text{RSTO}}$, and $\overline{\text{RSTO}}$ remains asserted for at least 31 clocks after the negation of $\overline{\text{RSTI}}$. $\overline{\text{RSTO}}$ will also be asserted for at least 31 clocks on a software watchdog time-out that is programmed to generate a reset.

2.8 DRAM CONTROLLER SIGNALS

The following DRAM signals provide a glueless interface to external DRAM:

2.8.1 Row Address Strobes ($\overline{\text{RAS[1:0]}}$)

These active-low output signals provide control for the row address strobe ($\overline{\text{RAS}}$) input pins on industry-standard DRAMs. There is one $\overline{\text{RAS}}$ output for each DRAM bank: $\overline{\text{RAS[0]}}$ controls DRAM bank 0 and $\overline{\text{RAS[1]}}$ controls DRAM bank 1. You can customize $\overline{\text{RAS}}$ timing to match the specifications of the DRAM being used by programming the DRAMC Timing Register (see **Section 10.4.2.2 DRAM Controller Timing Register (DCTR)).**

2.8.2 Column Address Strobes ($\overline{\text{CAS[3:0]}}$)

These active-low output signals provide control for the column address strobe ($\overline{\text{CAS}}$) input pins on industry-standard DRAMs. The $\overline{\text{CAS}}$ signals enable data byte lanes: $\overline{\text{CAS[0]}}$ controls access to D[31:24], $\overline{\text{CAS[1]}}$ to D[23:16], $\overline{\text{CAS[2]}}$ to D[15:8], and $\overline{\text{CAS[3]}}$ to D[7:0].

You should use $\overline{CAS}[3:0]$ for a 32-bit wide DRAM bank, $\overline{CAS}[1:0]$ for a 16-bit wide DRAM bank, and $\overline{CAS}[0]$ for an 8-bit wide DRAM bank. Table 2-9 shows which $\overline{CAS}$ signals are asserted based on the operand size, the DRAM port size, and the address bits A[1:0]. You can customize $\overline{CAS}$ timing to match the specifications of the DRAM by programming the DRAM Controller Timing Register (see **Section 10.4.2.2 DRAM Controller Timing Register (DCTR)**).

Table 2-9. $\overline{CAS}$ Assertion

OPERAND SIZE	PORT SIZE	SIZ[1]	SIZ[0]	A[1]	A[0]	$\overline{CAS}[0]$	$\overline{CAS}[1]$	$\overline{CAS}[2]$	$\overline{CAS}[3]$
						D[31:24]	D[23:16]	D[15:8]	D[7:0]
BYTE	8-bit	0	1	0	0	0	1	1	1
				0	1	0	1	1	1
				1	0	0	1	1	1
				1	1	0	1	1	1
	16-bit	0	1	0	0	0	1	1	1
				0	1	1	0	1	1
				1	0	0	1	1	1
				1	1	1	0	1	1
	32-bit	0	1	0	0	0	1	1	1
				0	1	1	0	1	1
				1	0	1	1	0	1
				1	1	1	1	1	0
WORD	8-bit	1	0	0	0	0	1	1	1
				0	1	0	1	1	1
				1	0	0	1	1	1
				1	1	0	1	1	1
	16-bit	1	0	0	0	0	0	1	1
				1	0	0	0	1	1
	32-bit	1	0	0	0	0	0	1	1
				1	0	1	1	0	0
LONG WORD	8-bit	0	0	0	0	0	1	1	1
				0	1	0	1	1	1
				1	0	0	1	1	1
				1	1	0	1	1	1
	16-bit	0	0	0	0	0	0	1	1
				1	0	0	0	1	1
	32-bit	0	0	0	0	0	0	0	0
LINE	8-bit	1	1	0	0	0	1	1	1
				0	1	0	1	1	1
				1	0	0	1	1	1
				1	1	0	1	1	1
	16-bit	1	1	0	0	0	0	1	1
				1	0	0	0	1	1
	32-bit	1	1	0	0	0	0	0	0

2.8.3 DRAM Write ($\overline{\text{DRAMW}}$)

This active-low output signal is asserted during DRAM write cycles and negated during DRAM read cycles. The $\overline{\text{DRAMW}}$ signal is negated during refresh cycles and is provided (in addition to the R/$\overline{\text{W}}$ signal) to allow refreshes to occur during non-DRAM cycles (regardless of the state of the R/$\overline{\text{W}}$ signal). The R/$\overline{\text{W}}$ signal indicates the direction of all bus transfers, while $\overline{\text{DRAMW}}$ is valid only during DRAM transfers.

2.9 UART MODULE SIGNALS

The signals listed below transfer serial data between the two UART modules (UART1 and UART2) and external peripherals.

2.9.1 Receive Data (RxD[1], RxD[2])

These are the inputs on which serial data is received by the UART modules. RxD[1] corresponds to UART1 and RxD[2] corresponds to UART2. Data is sampled on RxD[1] and RxD[2] on the rising edge of the serial clock source, with the least significant bit received first.

2.9.2 Transmit Data (TxD[1], TxD[2])

The UART modules transmit serial data on these outputs. TxD[1] corresponds to UART1 and TxD[2] corresponds to UART2. Data is transmitted on the falling edge of the serial clock source, with the least significant bit (LSB) transmitted first. When no data is being transmitted or the transmitter is disabled, these two signals are held high. TxD[1] and TxD[2] are also held high in local loopback mode.

2.9.3 Request To Send ($\overline{\text{RTS[1]}}$, $\overline{\text{RTS[2]}}$/$\overline{\text{RSTO}}$)

$\overline{\text{RTS[2]}}$ is multiplexed with the $\overline{\text{RSTO}}$ signal. Programming the Pin Assignment Register (PAR) in the SIM determines the function of this pin. During reset, this pin is configured to be $\overline{\text{RSTO}}$.

The request-to-send output indicates to the peripheral device that the UART module is ready to receive data. $\overline{\text{RTS[1]}}$ corresponds to UART1 and $\overline{\text{RTS[2]}}$ corresponds to UART2.

2.9.4 Clear To Send ($\overline{\text{CTS[1]}}$, $\overline{\text{CTS[2]}}$)

Peripherals drive these inputs to indicate to the UART module that it can begin data transmission. $\overline{\text{CTS[1]}}$ corresponds to UART1 and $\overline{\text{CTS[2]}}$ corresponds to UART2.

2.10 TIMER MODULE SIGNALS

The signal descriptions that follow are the external interface to the two general-purpose timer modules (Timer1 and Timer2).

2.10.1 Timer Input (TIN[2], TIN[1])

You can program the timer input to be the clock for the timer module. You can also program the timer module to trigger a capture on the rising edge, falling edge, or both edges of the timer input. TIN[1] corresponds to Timer1 and TIN[2] corresponds to Timer2.

2.10.2 Timer Output (TOUT[2], TOUT[1])

The programmable timer output pulses or toggles when the timer reaches the programmed count value. TOUT[1] corresponds to Timer1 and TOUT[2] corresponds to Timer2.

2.11 M-BUS MODULE SIGNALS

The M-Bus module acts as quick two-wire, bidirectional serial interface between the MCF5206 and peripherals with an M-Bus interface (e.g., LED controller, A-to-D converter, D-to-A converter). All devices connected to the M-Bus must have open-drain or open-collector outputs.

2.11.1 M-Bus Serial Clock (SCL)

This bidirectional, open-drain signal is the clock signal for M-Bus module operation. It is controlled by the M-Bus module when the bus is in master mode; all M-Bus devices drive this signal to synchronize M-Bus timing.

2.11.2 M-Bus Serial Data (SDA)

This bidirectional, open-drain signal is the data input/output for the serial M-Bus interface.

2.12 GENERAL-PURPOSE I/O SIGNALS

2.12.1 General-Purpose I/O (PP[7:4]/PST[3:0])

These general-purpose I/O signals are multiplexed with the processor status signals, PST[3:0]. Programming the Pin Assignment Register (PAR) in the SIM determines the function of these pins. During reset, these pins are configured as general-purpose inputs.

When programmed as general-purpose I/O, you can configure these signals as inputs or outputs and they can be asserted and negated through programmable control.

2.12.2 Parallel Port (General-Purpose I/O) (PP[3:0]/DDATA[3:0])

These programmable parallel port signals are multiplexed with the debug data signals, DDATA[3:0]. Programming the Pin Assignment Register (PAR) in the SIM determines the function of these pins. During reset, these pins are configured as general-purpose inputs.

When programmed as general-purpose I/O, you can configure these signals as inputs or outputs and they can be asserted and negated through programmable control.

2.13 DEBUG SUPPORT SIGNALS

2.13.1 Processor Status (PP[7:4]/PST[3:0])

The processor status signals are multiplexed with general-purpose I/O signals. Programming the Pin Assignment Register (PAR) in the SIM determines the function of these pins. During reset, these pins are configured as general-purpose inputs.

These outputs indicate the MCF5206 processor status. During debug mode, the timing is synchronous with the processor clock (CLK) and the status is not related to the current bus transfer. Table 2-10 shows the encodings of PST[3:0].

Table 2-10. Processor Status Encodings

HEX	PST[3:0] BINARY	DEFINITION
$0	0000	Continue execution
$1	0001	Begin execution of an instruction
$2	0010	Reserved
$3	0011	Entry into user-mode
$4	0100	Begin execution of **PULSE** instruction
$5	0101	Begin execution of taken branch
$6	0110	Reserved
$7	0111	Begin execution of **RTE** instruction
$8	1000	Reserved
$9	1001	Reserved
$A	1010	Reserved
$B	1011	Reserved
$C	1100	† Exception processing
$D	1101	† Emulator-mode entry exception processing
$E	1110	† Processor is stopped, waiting for interrupt
$F	1111	† Processor is halted
	† These encodings are asserted for multiple cycles.	

2.13.2 Debug Data (PP[3:0]/DDATA[3:0])

The debug data signals are multiplexed with general-purpose I/O signals. Programming the Pin Assignment Register (PAR) in the SIM determines the function of these pins. During reset, these pins are configured as general-purpose inputs.

The DDATA[3:0] outputs display captured processor data and break-point status. See the **Debug Support** section for additional information on this bus.

2.13.3 Development Serial Clock ($\overline{\text{TRST}}$/DSCLK)

The MTMOD signal determines the function of this dual-purpose pin. If MTMOD= 0, the $\overline{\text{TRST}}$ function is selected. If MTMOD=1, the DSCLK function is selected. MTMOD should not be changed while $\overline{\text{RSTI}}$ = 1.

The DSCLK input signal is used as the development serial clock for the serial interface to the debug module.The maximum frequency for the DSCLK signal is 1/2 the CLK frequency. See the **Debug Support** section for additional information on this signal.

2.13.4 Break Point (TMS/$\overline{\text{BKPT}}$)

The MTMOD signal determines the function of this dual-purpose pin. If MTMOD = 0, then the TMS function is selected. If MTMOD =1, the $\overline{\text{BKPT}}$ function is selected. MTMOD should not change while $\overline{\text{RSTI}}$ = 1.

The assertion of the active-low $\overline{\text{BKPT}}$ input signal causes a hardware breakpoint to occur in the processor when in the debug mode. See the **Debug Support** section for additional information on this signal.

2.13.5 Development Serial Input (TDI/DSI)

The MTMOD signal determines the function of this dual-purpose pin. If MTMOD = 0, then TDI is selected. If MTMOD = 1, then DSI is selected. MTMOD should not change while $\overline{\text{RSTI}}$ = 1.

The DSI input signal is the serial data input for the Debug module commands. See the **Debug Support** section for additional information on this signal.

2.13.6 Development Serial Output (TDO/DSO)

The MTMOD signal determines the function of this dual-purpose pin. When MTMOD = 0, TDO is selected. When MTMOD = 1, then DSO is selected. MTMOD should not change while $\overline{\text{RSTI}}$ = 1.

The DSO output signal is the serial data output for the debug module responses. See the **Debug Support** section for additional information on this signal.

2.14 JTAG SIGNALS

2.14.1 Test Clock (TCK)

TCK is the dedicated JTAG test logic clock that is independent of the MCF5206 processor clock. The internal JTAG controller logic is designed such that holding TCK high or low for an indefinite period of time will not cause the JTAG test logic to lose state information. TCK should be grounded if it is not used.

2.14.2 Test Reset ($\overline{\text{TRST}}$/DSCLK)

The MTMOD signal determines the function of this dual-purpose pin. If MTMOD= 0, the TRST function is selected. If MTMOD=1, the DSCLK function is selected. MTMOD should not be changed while $\overline{\text{RSTI}}$ = 1.

The assertion of the active-low $\overline{\text{TRST}}$ input pin will asynchronously reset the JTAG TAP controller to the test logic reset state, causing the JTAG instruction register to choose the

‘‘bypass’’ command. When this occurs, all the JTAG logic is benign and will not interfere with the normal functionality of the MCF5206 processor. Although this signal is asynchronous, we recommend that $\overline{\text{TRST}}$ make only a 0 to 1 (asserted to negated) transition while TMS is held at a logic 1 value. $\overline{\text{TRST}}$ has an internal pullup so that if it is not driven low, its value will default to a logic level of 1. However, if JTAG will not be used, $\overline{\text{TRST}}$ can either be tied to ground, placing the JTAG controller in the test logic reset state immediately, or tied to VDD, causing the JTAG controller (if TMS is a logic 1) to eventually end up in the test logic reset state after five clocks of TCK.

2.14.3 Test Mode Select (TMS/$\overline{\text{BKPT}}$)

The MTMOD signal determines the function of this dual-purpose pin. If MTMOD = 0, then the TMS function is selected. If MTMOD =1, the BKPT function is selected. MTMOD should not change while $\overline{\text{RSTI}}$ = 1.

The TMS input signal provides the JTAG controller with information to determine which test operation should be performed. The value of TMS and the current state of the internal 16-state JTAG controller state machine at the rising edge of TCK determine whether the JTAG controller holds its current state or advances to the next state. This directly controls whether JTAG data or instruction operations occur. TMS has an internal pullup so that if it is not driven low, its value will default to a logic level of 1. However, if TMS will not be used, it should be tied to VDD.

2.14.4 Test Data Input (TDI/DSI)

The MTMOD signal determines the function of this dual-purpose pin. If MTMOD = 0, then TDI is selected. If MTMOD = 1, then DSI is selected. MTMOD should not change while $\overline{\text{RSTI}}$ = 1.

The TDI input signal provides the serial data port for loading the various JTAG shift registers (the boundary scan register, the bypass register, and the instruction register). Shifting in of data depends on the state of the JTAG controller state machine and the instruction currently in the instruction register. This data shift occurs on the rising edge of TCK. TDI also has an internal pullup so that if it is not driven low, its value will default to a logic level of 1. However, if TDI will not be used, it should be tied to VDD.

2.14.5 Test Data Output (TDO/DSO)

The MTMOD signal determines the function of this dual-purpose pin. When MTMOD = 0, TDO is selected. When MTMOD = 1, then DSO is selected. MTMOD should not change while $\overline{\text{RSTI}}$ = 1.

The TDO output signal provides the serial data port for outputting data from the JTAG logic. Shifting out of data depends on the state of the JTAG controller state machine and the instruction currently in the instruction register. This data shift occurs on the falling edge of TCK. When TDO is not outputting test data, it is placed in a high-impedence state. TDO can also be three-stated to allow bussed or parallel connections to other devices having JTAG.

2.15 TEST SIGNALS

2.15.1 Motorola Test Mode (MTMOD)

This input signal chooses between the debug and JTAG signals that are multiplexed together. When MTMOD=1, the MCF5206 is in debug mode and when MTMOD=0, the MCF5206 is in JTAG mode.

2.15.2 High Impedance ($\overline{HIZ}$)

The assertion of the $\overline{HIZ}$ input signal will force all output drivers to a high-impedance state (three-state). The timing on $\overline{HIZ}$ is independent of the clock. Note that $\overline{HIZ}$ does not override JTAG operation; TDO/DSO can be forced to a high-impedance state by asserting $\overline{TRST}$.

If $\overline{RSTI}$ and $\overline{HIZ}$ are asserted simultaneously, the MCF5206 enters master reset mode. In this reset mode, the entire MCF5206 (including the DRAM controller refresh circuitry) is reset. You must use master reset for all power-on resets.

If $\overline{RSTI}$ is asserted while $\overline{HIZ}$ is negated, the MCF5206 enters normal reset mode. In this reset mode, the DRAM controller refresh circuitry will not be reset and will continue to generate refresh cycles at the programmed rate.

2.16 SIGNAL SUMMARY

Table 2-11 provides a summary of the electrical characteristics of the MCF5206 signals.

Table 2-11. MCF5206 Signal Summary

SIGNAL NAME	MNEMONIC	INPUT/OUTPUT	ACTIVE STATE	RESET STATE
Address[27:24]/Chip-Select[7:4]/ Write Enable[0:3]	A[27:24]/ $\overline{CS}$[7:4]/ $\overline{WE}$[0:3]	In,Out/ Out/ Out	-/ Low/ Low	Three-state/ Negated/ Negated
Address	A[23:0]	In,Out	-	Three-stated
Data	D[31:0]	In,Out	-	Three-stated
Chip-Select[3:0]	$\overline{CS}$[3:0]	Out	Low	Negated
Interrupt Priority Level/ Interrupt Request	$\overline{IPL}$[2]/$\overline{IRQ}$[7] $\overline{IPL}$[1]/$\overline{IRQ}$[4] $\overline{IPL}$[0]/$\overline{IRQ}$[1]	In/In	Low	-
Read/Write	R/$\overline{W}$	In,Out	-	Three-stated
Size	SIZ[1:0]	In,Out	-	Three-stated
Transfer Type	TT[1:0]	Out	-	Three-stated
Access Type & Mode	ATM	Out	-	Three-stated
Transfer Start	$\overline{TS}$	In,Out	Low	Three-stated
Transfer Acknowledge	$\overline{TA}$	In,Out	Low	Three-stated
Asynchronous Transfer Acknowledge	$\overline{ATA}$	In	Low	-
Transfer Error Acknowledge	$\overline{TEA}$	In	Low	-
Bus Request	$\overline{BR}$	Out	Low	Negated
Bus Grant	$\overline{BG}$	In	Low	-

Table 2-11. MCF5206 Signal Summary (Continued)

SIGNAL NAME	MNEMONIC	INPUT/OUTPUT	ACTIVE STATE	RESET STATE
Bus Driven	$\overline{BD}$	Out	Low	Negated
Clock Input	CLK	In	-	-
Reset	$\overline{RSTI}$	In	Low	-
Row Address Strobe	$\overline{RAS}$[1:0]	Out	Low	Master Reset - Negated Normal Reset - Unaffected
Column Address Strobe	$\overline{CAS}$[3:0]	Out	Low	Master Reset - Negated Normal Reset - Unaffected
DRAM Write	$\overline{DRAMW}$	Out	Low	Negated
Receive Data	RxD[1], RxD[2]	In	-	-
Transmit Data	TxD[1], TxD[2]	Out	-	Asserted
Request-To-Send	$\overline{RTS}$[1]	Out	Low	Negated
Request-To-Send	$\overline{RTS}$[2]/ $\overline{RSTO}$	Out/ Out	Low/ Low	Asserted
Clear-To-Send	$\overline{CTS}$[1], $\overline{CTS}$[2]	In	Low	-
Timer Input	TIN[1], TIN[2]	In	-	-
Timer Output	TOUT[1], TIN[2]	Out	-	Asserted
Serial Clock Line	SCL	In,Out	Low	Negated
Serial Data Line	SDA	In,Out	Low	Negated
General Purpose I/O/ Processor Status	PP[7:4]/ PST[3:0]	In.Out/ Out	-/ -	Three-stated
General Purpose I/O/ Debug Data	PP[3:0]/ DDATA[3:0]	In,Out/ Out	-/ -	Three-stated
Test Clock	TCK	In	-	-
Test Data Output/Development Serial Output	TDO/ DSO	Out/ Out	-/ -	Three-Stated/ Negated
Test Mode Select/ Break Point	TMS/ $\overline{BKPT}$	In/ In	-/ Low	-/ -
Test Data Input / Development Serial Input	TDI/ DSI	In/ In	-/ -	-/ -
Test Reset/Development Serial Clock	$\overline{TRST}$/ DSCLK	In/ In	Low/ -	-/ -
Motorola Test Mode	MTMOD	In	-	-
High Impedance	$\overline{HIZ}$	In	Low	-