SECTION 9
PARALLEL PORT (GENERAL-PURPOSE I/O) MODULE

9.1 INTRODUCTION

The MCF5206 provides eight general-purpose input/output signals that can be used on a pin-by-pin basis. This subsection describes the operation and programming model of the parallel port registers and the direction-control and data registers.

9.2 PARALLEL PORT OPERATION

The MCF5206 parallel port module has eight signals that you can select as inputs or outputs on a pin-by-pin basis. These pins are multiplexed with the MCF5206 emulation pins and are programmed to their parallel port function through the Pin Assignment Register (PAR). Refer to the SIM subsection **6.3.2.10 Pin Assignment Register** for programming description.

9.3 PROGRAMMING MODEL

9.3.1 Parallel Port Registers Memory Map

Table 9-1 shows the memory map of all the parallel port registers. The internal registers in the parallel port module are memory-mapped registers offset from the MBAR address pointer. Refer to the SIM section for programming of the MBAR.

The following key notes apply to the programming model table:

- Addresses not assigned to a register and undefined register bits are reserved for future expansion. Write accesses to these reserved address spaces and reserved register bits have no effect; read accesses will return zeros.
- The reset value column indicates the register initial value at reset. Certain registers can be uninitialized at reset.
- The access column indicates if the corresponding register allows both read/write functionality (R/W), read-only functionality (R), or write-only functionality (W). Any read-access attempts to a write-only register will return zeros. A write access to a read-only register attempt will be ignored and no write will occur.

Table 9-1. Memory Map of Parallel Port Registers

ADDRESS	NAME	WIDTH	DESCRIPTION	RESET VALUE	ACCESS
MBAR + $1C5	PPDDR	8	Port A Data Direction Register	$00	R/W
MBAR + $1C9	PPDAT	8	Port A Data Register	$00	R/W

9.3.2 Parallel Port Registers

9.3.2.1 PORT A DATA DIRECTION REGISTER (PADDR). The data direction register allows you to select the signal direction of each parallel port signal. There is one DDR bit in the PADDR for each parallel port signal. The data direction control bits will only affect the direction of the associated pin if you program that pin as a general- purpose I/O signal in the PAR. Refer to SIM subsection **6.3.2.10 Pin Assigment Register(PAR)** for programming details.

The DDR is an 8-bit read/write register. At system reset, all bits are initialized to zero.

Data Direction Register (DDR) — Address MBAR + $1C5

7	6	5	4	3	2	1	0
DDR7	DDR6	DDR5	DDR4	DDR3	DDR2	DDR1	DDR0
RESET: 0	0	0	0	0	0	0	0
R/W							

DDR[7:0] - Data Direction Bits[7:0]

For each of the data direction bits, you can select the direction of the signal as follows:

0 = Signal is an input
1 = Signal is an output

Table 9-1 indicates how the bits in the data direction register are assigned to the PP[7:4]/ DDATA[3:0] and PP[3:0]/PST[3:0] signal pins.

Table 9-1. Data Direction Register Bit Assignments

DATA DIRECTION REGISTER BIT	OUTPUT PIN
DDR7	PP[7]/DDATA[3]
DDR6	PP[6]/DDATA[2]
DDR5	PP[5]/DDATA[1]
DDR4	PP[4]/DDATA[0]
DDR3	PP[3]/PST[3]
DDR2	PP[2]/PST[2]
DDR1	PP[1]/PST[1]
DDR0	PP[0]/PST[0]

9.3.2.2 PORT A DATA REGISTER (PADAT). The parallel port data register reflects the current status of the parallel port signals. If you configure a parallel port signal as an input, the value in the register corresponds to the logical voltage level present at the pin. If you configure the parallel portsignal as an output, the value in the register corresponds to the logical voltage level driven onto the pin.

The Parallel Port Data Register is an 8-bit read/write register. At system reset, the PADAT is initialized to zeros.

Parallel Port Data Register(PPDAT) Address MBAR + $1C9

7	6	5	4	3	2	1	0
DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0
RESET: 0	0	0	0	0	0	0	0
R/W							

NOTE

Bits in PADAT are valid for the pins configured as general-purpose I/O only. If you configure a pin to output Background Debug mode signals, the value of PADAT will not be valid.

NOTE

You can write to the PADAT register at anytime. A write to a bit corresponding to an input signal will seemingly have no affect. However, if a pin change from an input to an output, the value most recently WRITTEN into the PADAT will be the value driven onto the pin.

DAT[7:0] - Parallel Port Data Register bits[7:0]

Each bit in the Parallel Port Data Register corresponds to a particular signal pin as indicated in Table 9-2. The values in this register are controlled as follows:

- For parallel port signals programmed to outputs:
  - — For PADAT read: register bit indicates logical voltage level at the pin
  - — For PADAT write: drive indicated logical voltage level onto associated pin
- For parallel port signals programmed to inputs:
  - — For PADAT read: register bit indicates current logical voltage level of pin
  - — For PADAT write: has no affect unless pin direction is changed to output. Refer to the NOTE above.

Table 9-2. Data Register Bit Assignments

DATA REGISTER BITS	OUTPUT PIN
DAT7	PP[7]/DDATA[3]
DAT6	PP[6]/DDATA[2]
DAT5	PP[5]/DDATA[1]
DAT4	PP[4]/DDATA[0]
DAT3	PP[3]/PST[3]
DAT2	PP[2]/PST[2]
DAT1	PP[1]/PST[1]
DAT0	PP[0]/PST[0]