APPENDIX A
MCF5206 MEMORY MAP SUMMARY

This section is a summary chart of the entire memory map for the MCF5206.

Table A-1. MCF5206 User Programming Model

ADDRESS	NAME	WIDTH	DESCRIPTION	RESET VALUE	ACCESS
MOVEC with $C0F	MBAR	32	Module Base Address Register	uninitialized (except V=0)	W
MBAR + $003	SIMR	8	SIM Configuration Register	$C0	R/W
MBAR + $014	ICR1	8	Interrupt Control Register 1 - External IRQ1/IPL1	$04	R/W
MBAR + $015	ICR2	8	Interrupt Control Register 2 - External IPL2	$08	R/W
MBAR + $016	ICR3	8	Interrupt Control Register 3 - External IPL3	$0C	R/W
MBAR + $017	ICR4	8	Interrupt Control Register 4 - External IRQ4/IPL4	$10	R/W
MBAR + $018	ICR5	8	Interrupt Control Register 5 - External IPL5	$14	R/W
MBAR + $019	ICR6	8	Interrupt Control Register 6 - External IPL6	$18	R/W
MBAR + $01A	ICR7	8	Interrupt Control Register 7 - External IRQ7/IPL7	$1C	R/W
MBAR + $01B	ICR8	8	Interrupt Control Register 8 - SWT	$1C	R/W
MBAR + $01C	ICR9	8	Interrupt Control Register 9 - Timer 1 Interrupt	$80	R/W
MBAR + $01D	ICR10	8	Interrupt Control Register 10 - Timer 2 Interrupt	$80	R/W
MBAR + $01E	ICR11	8	Interrupt Control Register 11 - MBUS Interrupt	$80	R/W
MBAR + $01F	ICR12	8	Interrupt Control Register 12 - UART 1 Interrupt	$00	R/W
MBAR + $020	ICR13	8	Interrupt Control Register 13 - UART2 Interrupt	$00	R/W
MBAR + $036	IMR	16	Interrupt Mask Register	$3FFE	R/W
MBAR + $03A	IPR	16	Interrupt Pending Register	$0000	R
MBAR + $040	RSR	8	Reset Status Register	$80 or $20	R/W
MBAR + $041	SYPCR	8	System Protection Control Register	$00	R/W
MBAR + $042	SWIVR	8	Software Watchdog Interrupt Vector Register	$0F	R/W
MBAR + $043	SWSR	8	Software Watchdog Service Register	uninitialized	W
MBAR + $046	DCRR	16	DRAM Controller Refresh	Master Reset: $0000 Normal Reset: uninitialized	R/W
MBAR + $04A	DCTR	16	DRAM Controller Timing Register	Master Reset: $0000 Normal Reset: uninitialized	R/W
MBAR + $04C	DCAR0	16	DRAM Controller Address Register - Bank 0	Master Reset: uninitialized Normal Reset: uninitialized	R/W
MBAR + $050	DCMR0	32	DRAM Controller Mask Register - Bank 0	Master Reset: uninitialized Normal Reset: uninitialized	R/W
MBAR + $057	DCCR0	8	DRAM Controller Control Register- Bank 0	Master Reset: $00 Normal Reset: $00	R/W
MBAR + $058	DCAR1	16	DRAM Controller Address Register - Bank 1	Master Reset: uninitialized Normal Reset: uninitialized	R/W

ADDRESS	NAME	WIDTH	DESCRIPTION	RESET VALUE	ACCESS
MBAR + $05C	DCMR1	32	DRAM Controller Mask Register - Bank 1	Master Reset: uninitialized Normal Reset: uninitialized	R/W
MBAR + $063	DCCR1	8	DRAM Controller Control Register - Bank 1	Master Reset: $00 Normal Reset: $00	R/W
MBAR + 64	CSAR0	16	Chip-Select Address Register - Bank 0	0000	R/W
MBAR + 68	CSMR0	32	Chip-Select Mask Register - Bank 0	00000000	R/W
MBAR + $06E	CSCR0	16	Chip-Select Control Register - Bank 0	3C1F, 3C5F, 3C9F, 3CDF, 3D1F, 3D5F, 3D9F, or 3DDF AA set by $\overline{IRQ7}$ at reset PS1 set by $\overline{IRQ4}$ at reset PS0 set by $\overline{IRQ1}$ at reset	R/W
MBAR + $070	CSAR1	16	Chip-Select Address Register - Bank 1	uninitialized	R/W
MBAR + $074	CSMR1	32	Chip-Select Mask Register - Bank 1	uninitialized	R/W
MBAR + $07A	CSCR1	16	Chip-Select Control Register - Bank 1	uninitialized (except BRST=ASET=WRAH=RDAH=WR=RD=0)	R/W
MBAR + $07C	CSAR2	16	Chip-Select Address Register - Bank 2	uninitialized	R/W
MBAR + $080	CSMR2	32	Chip-Select Mask Register - Bank 2	uninitialized	R/W
MBAR + $086	CSCR2	16	Chip-Select Control Register - Bank 2	uninitialized (except BRST=ASET=WRAH=RDAH=WR=RD=0)	R/W
MBAR + $088	CSAR3	16	Chip-Select Address Register - Bank 3	uninitialized	R/W
MBAR + $08C	CSMR3	32	Chip-Select Mask Register - Bank 3	uninitialized	R/W
MBAR + $092	CSCR3	16	Chip-Select Control Register - Bank 3	uninitialized (except BRST=ASET=WRAH=RDAH=WR=RD=0)	R/W
MBAR + $094	CSAR4	16	Chip-Select Address Register - Bank 4	uninitialized	R/W
MBAR + $098	CSMR4	32	Chip-Select Mask Register - Bank 4	uninitialized	R/W
MBAR + $09E	CSCR4	16	Chip-Select Control Register - Bank 4	uninitialized (except BRST=ASET=WRAH=RDAH=WR=RD=0)	R/W
MBAR + $0A0	CSAR5	16	Chip-Select Address Register - Bank 5	uninitialized	R/W
MBAR + $0A4	CSMR5	32	Chip-Select Mask Register - Bank 5	uninitialized	R/W
MBAR + $0AA	CSCR5	16	Chip-Select Control Register - Bank 5	uninitialized (except BRST=ASET=WRAH=RDAH=WR=RD=0)	R/W
MBAR + $0AC	CSAR6	16	Chip-Select Address Register - Bank 6	uninitialized	R/W
MBAR + $0B0	CSMR6	32	Chip-Select Mask Register - Bank 6	uninitialized	R/W
MBAR + $0B6	CSCR6	16	Chip-Select Control Register - Bank 6	uninitialized (except BRST=ASET=WRAH=RDAH=WR=RD=0)	R/W
MBAR + $0B8	CSAR7	16	Chip-Select Address Register - Bank 7	uninitialized	R/W
MBAR + $0BC	CSMR7	32	Chip-Select Mask Register - Bank 7	uninitialized	R/W
MBAR + $0C2	CSCR7	16	Chip-Select Control Register - Bank 7	uninitialized (except BRST=ASET=WRAH=RDAH=WR=RD=0)	R/W
MBAR + $0C6	DMCR	16	Default Memory Control Register	0000	R/W

ADDRESS	NAME	WIDTH	DESCRIPTION	RESET VALUE	ACCESS
MBAR + $0CB	PAR	8	Pin Assignment Register	$00	R/W
MBAR+$100	TMR1	16	Timer1 Mode Register	$0000	R/W
MBAR+$104	TRR1	16	Timer1 Reference Register	$FFFF	R/W
MBAR+$108	TCR1	16	Timer1 Capture Register	$0000	R
MBAR+$10C	TCN1	16	Timer1 Counter	$0000	R/W
MBAR+$111	TER1	8	Timer1 Event Register	$00	R/W
MBAR+$120	TMR2	16	Timer2 Mode Register	$0000	R/W
MBAR+$124	TRR2	16	Timer2 Reference Register	$FFFF	R/W
MBAR+$128	TCR2	16	Timer2 Capture Register	$0000	R
MBAR+$12C	TCN2	16	Timer2 Counter	$0000	R/W
MBAR+$131	TER2	8	Timer2 Event Register	$00	R/W
MBAR + $140	UMR1,2	8	UART1 Mode Registers	$00	R/W
MBAR+$144	USR/ UCSR	8	UART1 Status Register (R/W=1)/ UART1 Clock-Select Register (R/W=0)	USR=$00; UCSR=$DD	USR=R; UC-SR=W
MBAR+$148	UCR	8	UART1 Command Register	$00	W
MBAR+$14C	URB/UTB	8	UART1 Receive Buffer (R/W=1)/ UART1 Transmit Buffer (R/W=0)	URB=$FF; UTB=$00	URB=R; UTB=W
MBAR+$150	UIPCR/ UACR	8	UART Input Port Change Register (R/w=1);/ UART1 Auxilary Control Register (R/W=0)	UIPCR=$0F; UACR=$00	UIPCR=R; UACR=W;
MBAR+$154	UISR/ UIMR	8	UART1 Interrupt Status Register (R/W=1); UART1 Interrupt Mask Register (R/W=0)	UISR=$00; UIMR=$00	UISR=R; UIMR=W
MBAR+$158	UBG1	8	UART1 Baud Rate Generator Prescale MSB	uninitialized	W
MBAR+$15C	UBG2	8	UART1 Baud Rate Generator Prescale LSB	uninitialized	W
MBAR+$170	UIVR	8	UART1 Interrupt Vector Register	$0F	R/W
MBAR+$174	UIP	8	UART1 Input Port Register	$FF	R
MBAR+$178	UOP1	8	UART1 Output Port Bit Set CMD	UOP1[7:1]= undefined; UOP1=0	W
MBAR+$17C	UOP0	8	UART1 Output Port Bit Reset CMD	uninitialized	W
MBAR+$180	UMR1,2	8	UART2 Mode Registers	$00	R/W
MBAR+$184	USR/ UCSR	8	UART2 Status Register (R/W=1)/ UART1 Clock-Select Register (R/W=0)	USR=$00; UCSR=$DD	USR=R; UC-SR=W
MBAR+$188	UCR	8	UART2 Command Register	$00	W
MBAR+$18C	URB/UTB	8	UART2 Receive Buffer (R/W=1)/ UART1 Transmit Buffer (R/W=0)	URB=$FF; UTB=$00	URB=R; UTB=W
MBAR+$190	UIPCR/ UACR	8	UART2 Input Port Change Register (R/w=1);/ UART1 Auxilary Control Register (R/W=0)	UIPCR=$0F; UACR=$00	UIPCR=R; UACR=W;
MBAR+$194	UISR/ UIMR	8	UART2 Interrupt Status Register (R/W=1); UART1 Interrupt Mask Register (R/W=0)	UISR=$00; UIMR=$00	UISR=R; UIMR=W
MBAR+$198	UBG1	8	UART2 Baud Rate Generator Prescale MSB	uninitialized	R/W
MBAR+$19C	UBG2	8	UART2 Barud Rate Generator Prescale LSB	uninitialized	R/W
MBAR+$1B0	UIVR	8	UART2 Interrupt Vector Register	$0F	R/W
MBAR+$1B4	UIP	8	UART2 Input Port Register	$FF	R
MBAR+$1B8	UOP1	8	UART2 Output Port Bit Set CMD	UOP1[7:1]= undefined; UOP1=0	W
MBAR+$1BC	UOP0	8	UART2 Output Port Bit Reset CMD	uninitialized	W
MBAR + $1C5	PPDDR	8	Port A Data Direction Register	$00	R/W
MBAR + $1C9	PPDAT	8	Port A Data Register	$00	R/W
MBAR+$1E0	MADR	8	M-Bus Address Register	$00	R/W

ADDRESS	NAME	WIDTH	DESCRIPTION	RESET VALUE	ACCESS
MBAR+$1E4	MFDR	8	M-Bus Frequency Divider Register	$00	R/W
MBAR+$1E8	MBCR	8	M-Bus Control Register	$00	R/W
MBAR+$1EC	MBSR	8	M-Bus Status Register	$00	R/W
MBAR+$1F0	MBDR	8	M-Bus Data I/O Register	$00	R/W